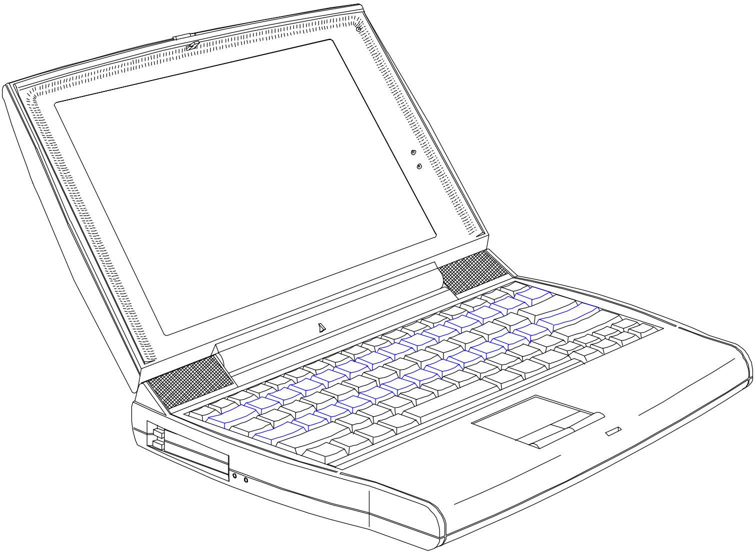
AcerNote 970

Service Guide



About this Manual

Purpose

This service guide contains reference information for the 370 notebook computer. It gives the system and peripheral specifications, shows how to identify and solve system problems and explains the procedure for removing and replacing system components. It also gives information for ordering spare parts.

Manual Structure

This service guide consists of four chapters and seven appendices as follows:

Chapter 1 Introduction

This chapter gives the technical specifications for the notebook and its peripherals.

Chapter 2 Major Chip Descriptions

This chapter lists the major chips used in the notebook and includes pin descriptions and related diagrams of these chips.

Chapter 3 BIOS Setup Information

This chapter includes the system BIOS information, focusing on the BIOS setup utility.

Chapter 4 Disassembly and Unit Replacement

This chapter tells how to disassemble the notebook and replace components.

Appendix A Model Number Definition

This appendix lists the model number definition of this notebook model series.

Appendix B Exploded View Diagram

This appendix shows the exploded view diagram of the notebook.

Appendix C Spare Parts List

This appendix contains spare parts information.

Appendix D Schematics

This appendix contains the schematic diagrams of the notebook.

Appendix E BIOS POST Checkpoints

This appendix lists all the BIOS POST checkpoints.

Appendix F Forms

This appendix contains standard forms that can help improve customer service.

Related product information

AcerNote 970 User's Manual contains system description and general operating instructions.

Vesuvius-LS Chipset Data Sheets contain information on the system core chips (V1-LS, V2-LS, V3-LS).

NMG2090 Data Sheet contains detailed information on the NeoMagic VGA controller.

RCV288Aci/SVD Chipset Data Sheet contains detailed information on the Rockwell Modem controller.

ESS1688W Data Sheet contains detailed information on the ESS audio controller.

87C552 Data Sheet contains detailed information on the Philips System Management Controller.

NS87336VLJ Data Sheet contains detailed information on the NS super I/O controller.

CL-PD6730 Data Sheet contains detailed information on the Cirrus Logic PCMCIA controller.

PCI0643 Data Sheets contain detailed information on the CMD PCI IDE controller.

T62.036.C , T62.039. and C T62.055.C Data Sheets contain detailed information on the Ambit components.

M38802 Data Sheet contains detailed information on the Phoenix keyboard controller.

Conventions

The following are the conventions used in this manual:

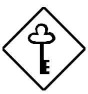
`Text entered by user`	Represents text input by the user.
`Screen messages`	Denotes actual messages that appear onscreen.
a, e, s, etc.	Represent the actual keys that you have to press on the keyboard.
	**NOTE** Gives bits and pieces of additional information related to the current topic.
	**WARNING** Alerts you to any damage that might result from doing or not doing specific actions.
	**CAUTION** Gives precautionary measures to avoid possible hardware or software problems.
	**IMPORTANT** Reminds you to do specific actions relevant to the accomplishment of procedures.
	**TIP** Tells how to accomplish a procedure with minimum steps through little shortcuts.

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Chapter 1 System Introduction

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Introduction

This chapter introduces the notebook computer, and describes its features and specifications.

1.1. Overview

This Pentium-based notebook computer combines high-performance, versatility, multimedia capabilities and a truly advanced power management system.

1.1.1 Features

PERFORMANCE

- Mobile Pentium microprocessor (P54CSLM-120/133/150)
- 64-bit DIMM memory architecture
- 256KB or 512 KB external (L2) cache memory
- Large display in DualScan STN(11.3”) or active-matrix TFT(11.8” or 12.1”)
- PCI local bus video with 128-bit graphics accelerator
- Flexible module bay (3.5-inch floppy drive or CD-ROM drive)
- High-capacity, Enhanced-IDE hard disk
- Heuristic power management with suspend-to-memory and zero-volt suspend-to-disk power-saving modes
- Lithium-Ion smart battery pack
- High speed connectivity
- 16-bit stereo audio with built-in FM synthesizer
- Built-in microphone and dual angled stereo speakers
- 30fps (frames per second) full-screen, true-color MPEG video playback
- Infrared wireless communication
- Internal 28.8Kbps modem with DSVD (digital simultaneous voice over data) support; with speakerphone and telephone answering device features

HUMAN-CENTRIC DESIGN AND ERGONOMICS

- Intuitive FlashStart automatic power-on

- Sleek, smooth and stylish design
- Automatic tilt-up, full-sized, full-function keyboard
- Wide and comfortable palm rest
- Ergonomically-centered touchpad pointing device

EXPANSION

- PC Card (formerly PCMCIA) slots (two type II/I or one type III)
- Mini dock option with built-in Ethernet
- User-upgradeable memory

1.1.2 FlashStart - Turning the Notebook Computer On and Off

A noticeably unique feature about this notebook is that it has no on/off switch. Instead it employs a lid switch, located near the center of the display hinge, that tells the notebook when it should wake up or go to sleep.

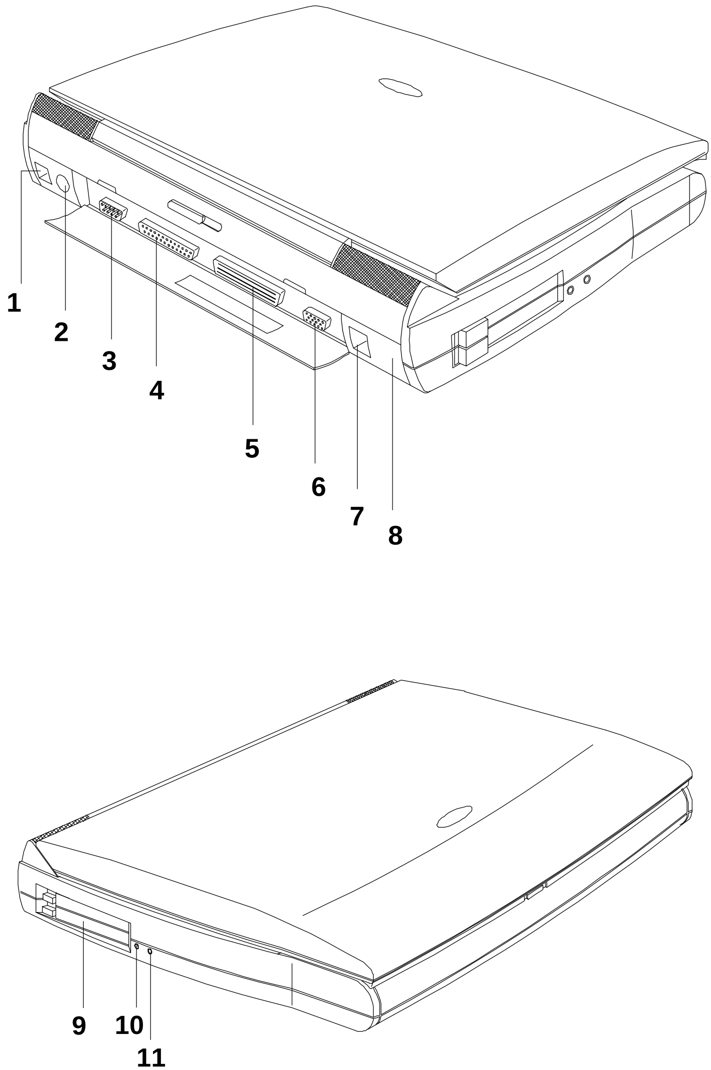
Figure 1- 1 FlashStart Automatic Power-on Switch (Lid Switch)

When you close the display lid, the notebook enters suspend-to-memory or suspend-to-disk mode before turning off the power, depending on the When Lid is Closed parameter setting in BIOS Setup. When you open the lid, the notebook resumes from where you left off before closing the lid.

Suspend-to-memory, suspend-to-disk and other power management issues are discussed in detail in power management section.

1.1.3 Ports

The notebook computer’s ports are found on the rear and left panel.



1	*DC-in Port*	*7*	*RJ-11 Phone Jack*
2	*PS/2 Port*	*8*	*Infrared Port*
3	*Serial Port*	*9*	*PC Card Slots*
4	*Parallel Port*	*10*	*Microphone-in/Line-in Jack*
5	*Mini Dock Connector*	*11*	*Speaker-out/Line-out Jack*
6	*External CRT Port*		

Figure 1- 2 Ports

The following table describes the ports.

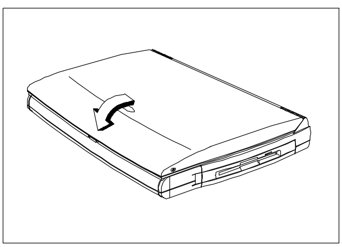
Table 1- 1 Port Descriptions

#	Icon	Port	Connects to...
Rear Panel Ports			
1		DC-in port	AC adapter and power outlet
2		PS/2 port	PS/2-compatible device (e.g., PS/2 keyboard, keypad, mouse)
3		Serial port (UART16650-compatible)	Serial device (e.g., serial mouse)
4		Parallel port (EPP/ECP-compliant)	Parallel device (e.g., parallel printer, floppy drive module when used externally)
5		Mini dock connector	Mini dock
6		External CRT port	External monitor (up to 1024x768, 256 colors)
7		Modem jack (RJ-11)	Phone line
8		Infrared port	Infrared-aware device (e.g., notebook with IR port, desktop with IR adapter, IR-capable printer)
Left Panel Ports			
9		PC Card slots	One Type III or two Type I/II PC cards
10		Microphone-in/Line-in	External microphone or line input device
11		Speaker-out/Line-out	Amplified speakers or headphones

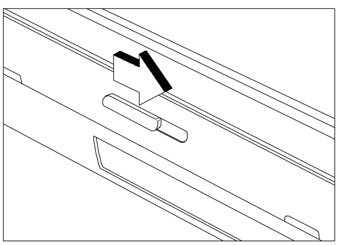
1.1.4 Automatic Tilt-up Keyboard

A tilt switch, found right above the port cover on the rear of the notebook, allows you to enable or disable this feature. Follow these steps:

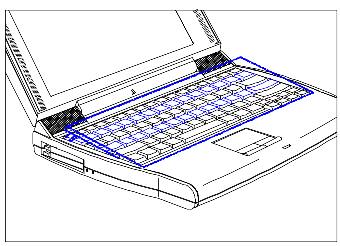
1. Close the lid.



2. To enable, slide the tilt switch to the right ( ). To disable, slide the tilt switch to the left ( ).



3. Open the lid.



1.1.5 Indicator Light

Two indicator lights are found on the display panel.

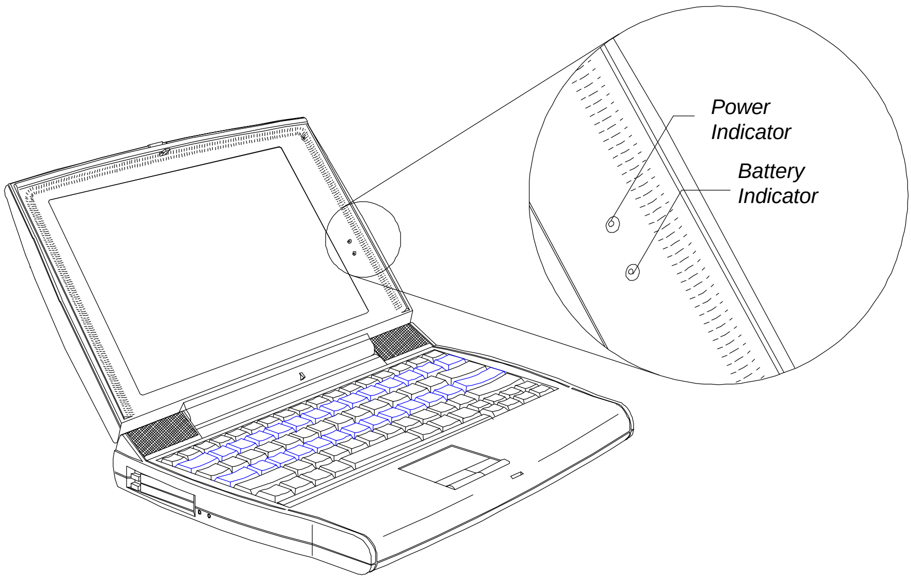


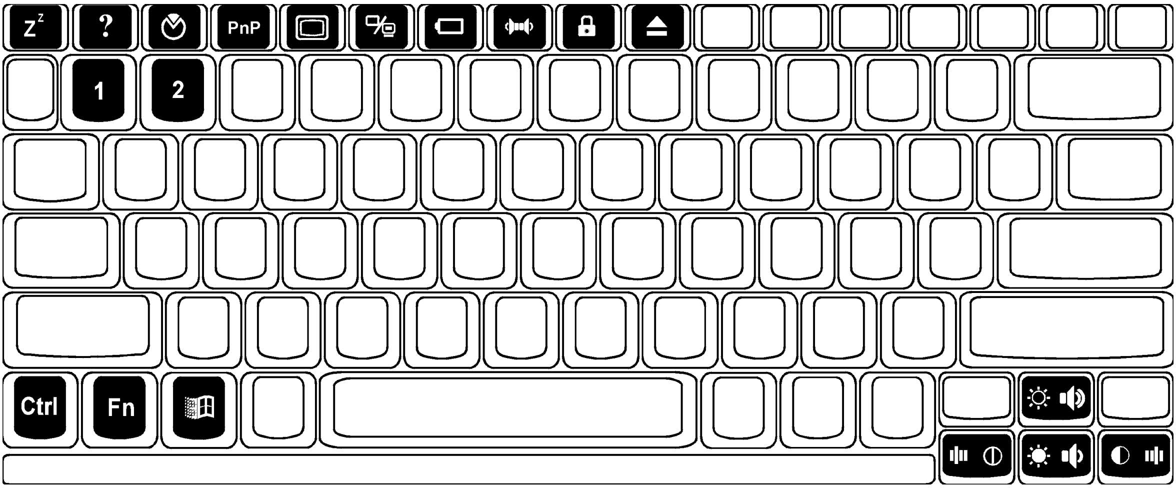
Figure 1- 3 Indicator Lights

These indicators and their descriptions are shown in the table below.

Table 1- 2 Indicator Status Descriptions

Icon	Indicator Light	Description
	Power Indicator	• Lights when power is on • Flashes when the notebook is in suspend-to-memory mode
	Battery Indicator	• Lights when battery pack is charging • Flashes when battery power is low

1.1.6 Keyboard Hotkey List

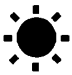


The following table lists and describes the hotkeys used by the notebook computer.

Table 1- 3 Hotkey List Descriptions

Hotkey	Icon	Function	Description
Fn-Esc		Suspend-to-memory	Enters suspend-to-memory mode
Fn-F1	?	Help	Displays the hotkey menu
Fn-F2		Setup	Enters the BIOS Setup utility
Fn-F3	PnP	Plug and Play Configuration	Allows the system to re-configure itself and do self-diagnostics
Fn-F4		Screen Blackout	Blanks the screen to save power. To wake up the screen, press any key.
Fn-F5		Display Toggle	Switches display from LCD to CRT to both LCD and CRT
Fn-F6		Fuel Gauge On/Off	Toggles battery gauge display on/off. Also shows the following: • "plug" icon if a powered AC adapter is connected to the notebook. • "speaker" icon if speaker output is on (toggled by Fn-F7). • "T" icon if turbo mode is on (toggled by Fn-2).
Fn-F7		Speaker On/Off	Toggles speaker output on and off
Fn-F8		Lock System Resources	Provides notebook security by locking system from access. Requires password input to unlock system.

Table 1- 3 Hotkey List Descriptions

Hotkey	Icon	Function	Description
Fn-F9		Eject	Accesses the Eject menu. See the following subsection.
Fn-Ctrl-↑		Volume Up	Increases audio volume
Fn-Ctrl-↓		Volume Down	Decreases audio volume
Fn-Ctrl-←		Balance Left	Shifts speaker balance to the left
Fn-Ctrl-→		Balance Right	Shifts speaker balance to the right
Fn-⊞-↑		Brightness Up	Increases screen brightness
Fn-⊞-↓		Brightness Down	Decreases screen brightness to save power
Fn-⊞-→		Contrast Up	Increases screen contrast (DSTN only)
Fn-⊞-←		Contrast Down	Decreases screen contrast (DSTN only)
Fn-↑		Fuel Gauge Up	With the fuel gauge onscreen, moves the fuel gauge up
Fn-↓		Fuel Gauge Down	With the fuel gauge onscreen, moves the fuel gauge down
Fn-←		Fuel Gauge Left	With the fuel gauge onscreen, moves the fuel gauge left
Fn-→		Fuel Gauge Right	With the fuel gauge onscreen, moves the fuel gauge right
Fn-1		CD Eject	Ejects the CD-ROM drive
Fn-2		Turbo Mode On/Off	Toggles turbo mode on and off.

1.1.6.1 Using the Eject Menu

Pressing **Fn-F9** brings up the Eject Menu.

```
                         Eject Menu

    Battery (Suspend to Disk)..............  Change
    CD-ROM Disc (Also Fn+1)................
    Power Off (Also Fn+BackSpace x3).......







       ↑↓ = Move Highlight Bar, ↲ = Select, Esc = Exit
```

The eject menu commands allow you to perform various eject-related functions for the notebook. See the following table for details

Table 1- 4 Eject Menu Descriptions

Select…	To…
Battery	Change the battery. This option forces the notebook to enter suspend-to-disk mode, so that you can replace the battery with a charged one, and then return to where you left off. To resume, close the display lid and open the display lid again.
CD-ROM Disc	Open the CD-ROM drive. There are many ways to open the CD-ROM disc tray: • selecting this option • pressing Fn-1 • pressing the CD-ROM eject button • using software controls It is best to wait for the CD-ROM light (found on the CD-ROM eject button) to go off before ejecting the CD-ROM drive.
Power Off	Turn the system off (without entering suspend-to-disk mode). When you choose this option, a “cold boot” occurs after re-starting the system (opening and closing the display). You can choose this option when you want to swap modules, or when you want to turn off the notebook without entering any of the suspend modes. To turn the notebook back on, close the display lid and open the display lid again.

1.2. System Specification Overview

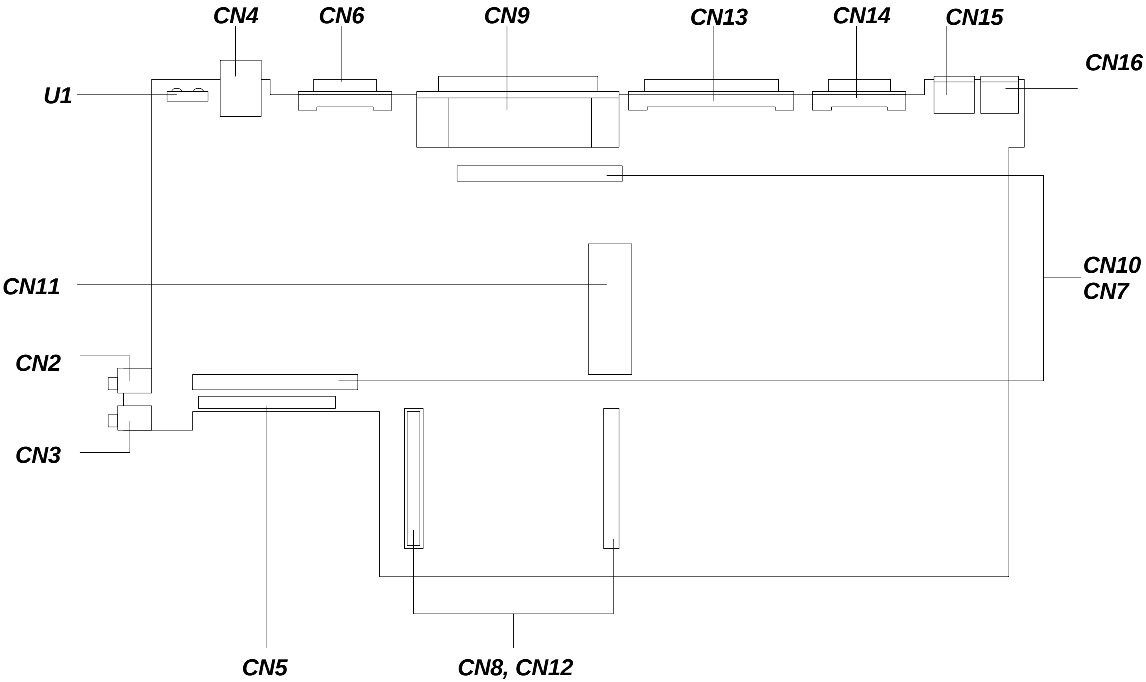
Table 1- 5 System Specifications

Item	Standard	Optional
Microprocessor	Mobile Intel Pentium™ processor (133/150MHz)	
Memory System / Main External cache	 16MB Dual 64-bit memory banks 256KB L2 cache (synchronous SRAM)	 Expandable to 64MB using 8/16/32MB soDIMMs 512KB L2 cache
System BIOS	256KB (Boot Block Flash ROM)	
Storage system	One 2.5-inch, high-capacity Enhanced-IDE hard disk One high-speed IDE CD-ROM drive module One 3.5-inch, 1.44MB floppy drive module (internal/external use)	Higher-capacity E-IDE hard disk
Display	DualScan STN or active-matrix TFT LCD, 800x600, 64K colors (SVGA)	Up to 1024x768, 256-color ultra-VGA monitor LCD projection panel
Video system	PCI local bus video with 128-bit graphics accelerator	
Audio system	16-bit stereo audio with built-in FM synthesizer Built-in microphone and dual angled speakers	
Communications system	Built-in V.34 fax/data modem (28.8Kbps) with digital simultaneous voice over data (DSVD) support	PC card modem
Operating system	Windows 95	DOS and Windows 3.x, OS/2 Warp
Keyboard and pointing device	84-/85-key with Win95 keys; auto-tilt feature Touchpad (centrally-located on palm rest)	101-/102-key, PS/2-compatible keyboard or 17-key numeric keypad External serial or PS/2 mouse or similar pointing device
I/O ports	One 9-pin RS-232 serial port (UART16550-compatible) One 25-pin parallel port (EPP/ECP-compliant) One 15-pin CRT port	Serial mouse, printer or other serial devices Parallel printer or other parallel devices; floppy drive module (when used externally) Up to a 1024x768 ultra-VGA monitor

Table 1- 5 System Specifications

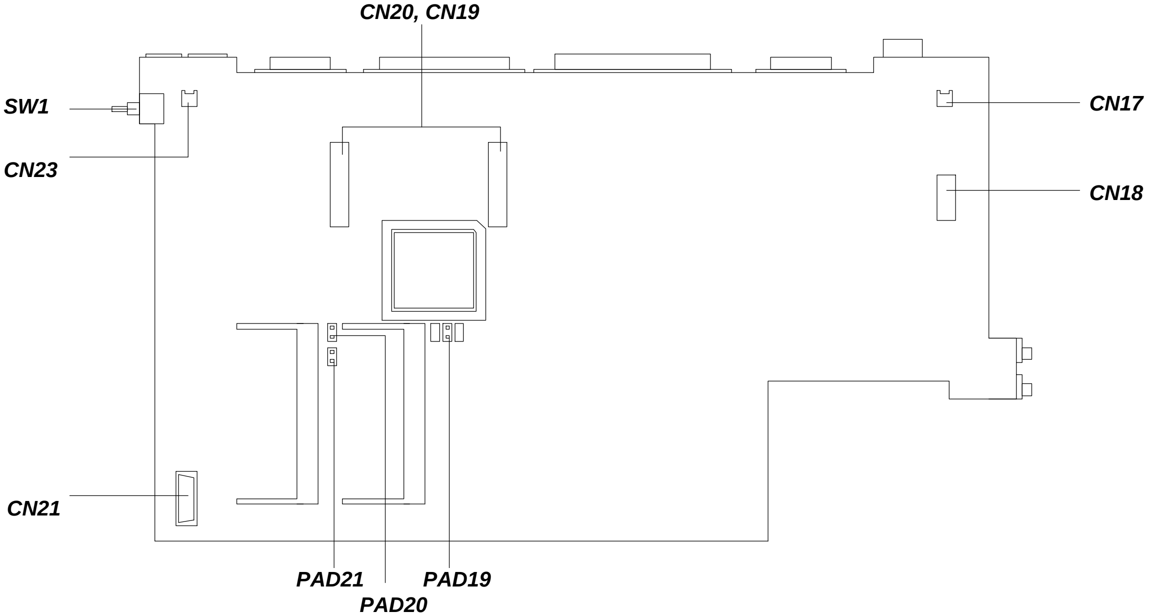
Item	Standard	Optional
	One 6-pin PS/2 connector One 240-pin mini dock connector One type III or two type II PC Card slot(s) One serial infrared port (IrDA-compliant) One 3.5mm minijack microphone-in/line-in jack One 3.5mm minijack speaker-out/line-out jack RJ11 phone jack	17-key numeric keypad, PS/2 keyboard, mouse or trackball Mini dock LAN card or other PC cards External IR devices and peripherals Microphone or line-in device Speakers or headphones
Weight with FDD with CD-ROM	(includes battery) 3.4 kg. (7.4 lbs.) 3.5 kg. (7.7 lbs.)	
Dimensions Round contour Main footprint	L x W x H 297~313mm x 230~240mm x 48~53mm 11.7” x 9.1” x 2”	Carrying bag
Temperature Operating Non-operating	 10ºC ~ 35ºC -10ºC ~ 60ºC	
Humidity Operating Non-operating	(non-condensing) 20% ~ 80% RH 20% ~ 80% RH	
AC adapter	100~240Vac, 50~60Hz autosensing AC adapter	Extra AC adapter
Battery pack Type Charge time	 58.3WH Lithium-Ion battery with intelligent charging and built-in battery gauge 2.0-hour rapid-charge 3.0-hour charge-in-use	Extra battery pack

1.4. Jumpers and Connectors



CN4	*Modem RJ11 phone jack*	*CN10, CN7*	*Multimedia board connector*
CN6	*VGA port*	*CN11*	*FDD/CD-ROM connector*
CN9	*Mini dock port*	*CN12, CN8*	*CPU board connector*
CN13	*Parallel port*	*CN5*	*Hard disk drive connector*
CN14	*Serial Port*	*CN3*	*Speaker-out/Line-out Jack*
CN15	*PS2 mouse/keyboard port*	*CN2*	*Microphone-in/Line-in Jack*
CN16	*AC adapter plug-in port*	*U1*	*SIR infrared LED*

Figure 1- 10 Mainboard Jumpers and Connectors (Top Side)

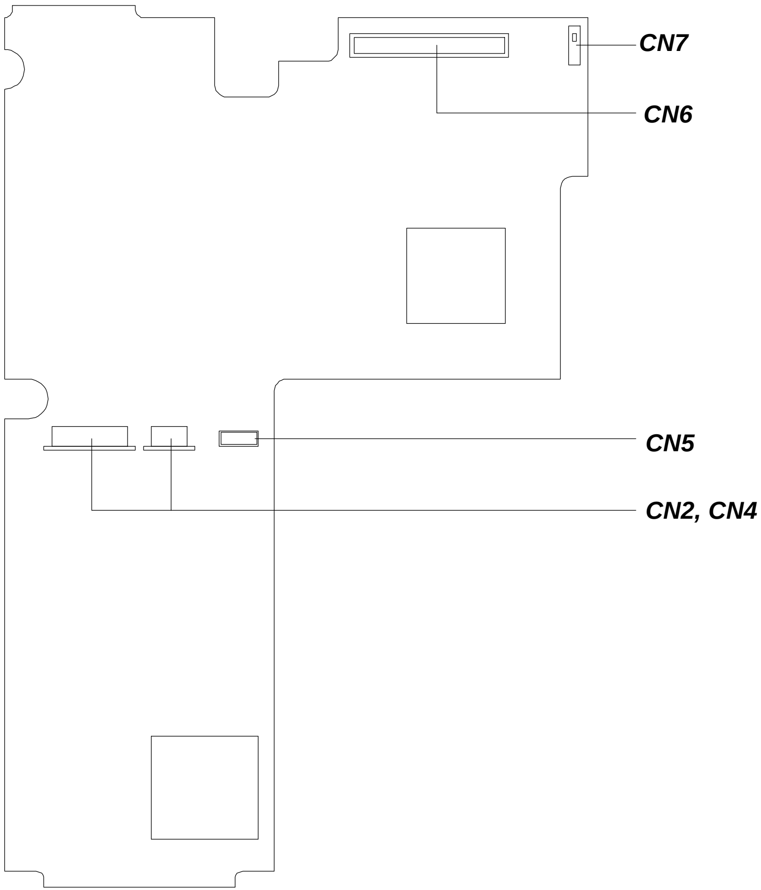


CN20, CN19 DC-DC converter connector
CN17 Left speaker connector
CN18 Debug port
PAD19 Keyboard type setting pad
PAD20 BIOS type setting pad
PAD21 Password setting pad
CN21 Battery connector
CN23 Right speaker connector
SW1 Reset Switch

Figure 1- 11 Mainboard Jumpers and Connectors (Bottom Side)

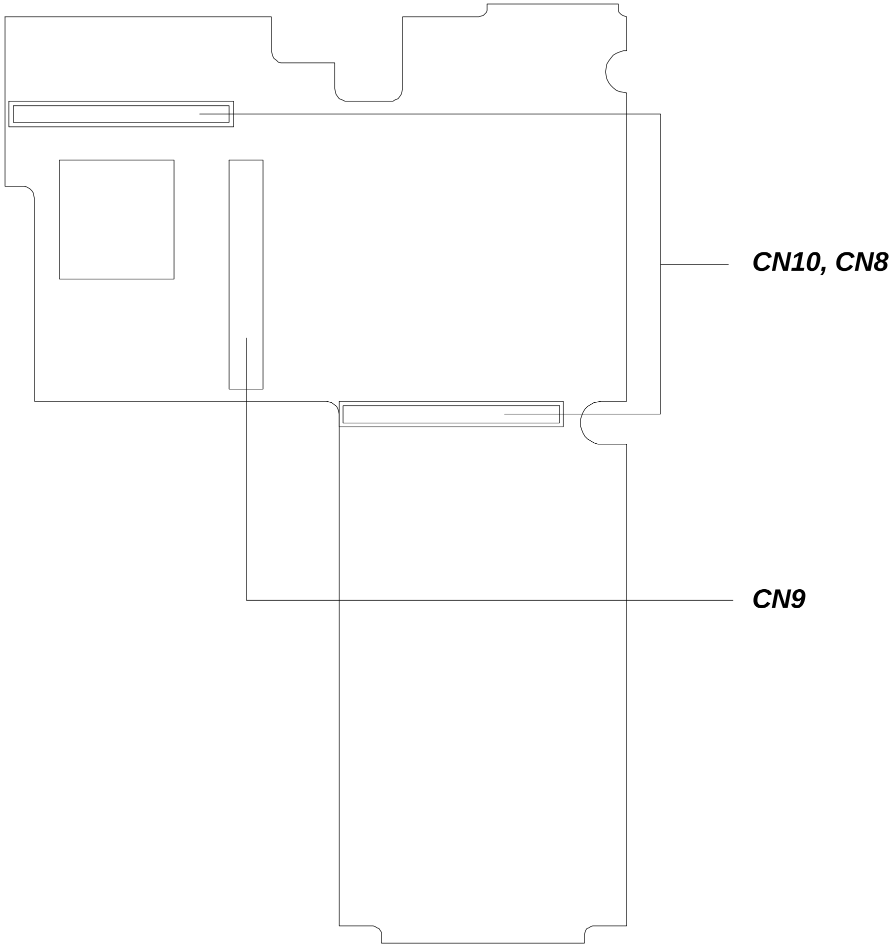
Table 1- 6 Mainboard Jumpers Pads Settings (Bottom Side)

Jumper Pad	Descriptions	Settings
PAD19	Keyboard type selection	Open: Other keyboard Short: Japan keyboard
PAD20	BIOS type selection	Open: Acer BIOS Short: OEM BIOS
PAD21	Password settings	Open: Enable password Short: Bypass password



CN7 Lid switch
CN6 LCD connector
CN5 Touchpad connector
CN4, CN2 Keyboard connector

Figure 1- 12 Media Board Jumpers and Connectors (Top Side)



CN10, CN8 Mainboard connector *CN9 PCMCIA socket connector*

Figure 1- 13 Media Board Jumpers and Connectors (Bottom Side)

1.5. System Configurations and Specifications

1.5.1 Memory Address Map

Table 1- 7 Memory Address Map

Address Range	Definition	Function
000000 - 09FFFF	640 KB memory	Base memory
0A0000 - 0BFFFF	128 KB video RAM	Reserved for graphics display buffer
0C0000 - 0CBFFF	Video BIOS	Video BIOS
0F0000 - 0FFFFF	64 KB system BIOS	System BIOS
100000 - top limited	Extended memory	SIMM memory
FE0000 - FFFFFF	256 KB system ROM	Duplicate of code assignment at 0E0000-0FFFFF

1.5.2 Interrupt Channel Map

Table 1- 8 Interrupt Channel Map

Interrupt Number	Interrupt Source (Device Name)
IRQ 0	System Timer
IRQ 1	Keyboard
IRQ 2	Cascade
IRQ 3	IrDA / 2F8h
IRQ 4	Serial Port 1 / 3F8h
IRQ 5	Audio ESS1688
IRQ 6	Floppy Disk Controller (FDC)
IRQ 7	Parallel Port
IRQ 8	Real Time Clock (RTC)
IRQ 9	Ethernet on Port Replicator
IRQ 10	Internal Modem / 3E8h
IRQ 11	PCMCIA
IRQ 12	PS/2 Mouse
IRQ 13	Co-processor
IRQ 14	Hard disk
IRQ 15	CD-ROM

1.5.3 I/O Address Map

Table 1- 9 I/O Address Map

Address Range	Device
000 - 00F	DMA controller-1
020 - 021	Interrupt controller-1
024, 026, B0h	PicoPower chipset registers
02E - 02F	CMD0643 IDE controller
040 - 043	Timer 1
048 - 04B	Timer 2
060 - 06E	Keyboard controller 8742 chip select
070 - 071	Real-time clock and NMI mask
080 - 08F	DMA page register
0A0 - 0A1	Interrupt controller-2
0C0 - 0DF	DMA controller-2
1F0 - 1F7	Hard disk select
3F6 - 3F7	Hard disk select
170 - 177	CD-ROM select
376 - 377	CD-ROM select
220 - 22F	Audio
240 - 24F	Audio - default
260 - 26F	Audio
280 - 28F	Audio
278 - 27F	Parallel port 3
2E8 - 2EF	COM 4
2F8 - 2FF	COM 2 - IrDA
300 - 301	MPU-401 port - default
310 - 311	MPU-401 port
320 - 321	MPU-401 port
330 - 321	MPU-401 port
34C - 34F	Docking station
378 - 37F	Parallel port 2
388 - 38B	FM synthesizer
3BC - 3BE	Parallel port 1
3B4, 3B5, 3BA	Video subsystem
3C0 - 3C5	
3C6 - 3C9	Video DAC
3C0 - 3CF	Enhanced graphics display
3D0 - 3DF	Color graphics adapter
3E8 - 3EF	COM3 - Modem
3F0 - 3F7	Floppy disk controller
3F8 - 3FF	COM 1 - Serial 1
CF8 - CFF	PCI configuration register

1.5.4 DMA Channel Map

Table 1- 10 DMA Channel Map

Controller	Channel	Address	Function
1	0	0087	Audio (default)
1	1	0083	Audio (option) / ECP
1	2	0081	Diskette
1	3	0082	Audio (option)
2	4	Cascade	Cascade
2	5	008B	
2	6	0089	Spare
2	7	008A	

1.5.5 GPIO Port Definition Map

Table 1- 11 GPIO Port Definition Map

GPIO	I/O	Description
V1-LS GPIO Pin Assignment		
PC0 (VS5_CLKEN)	O	1: Enable the clock source
PC1 (VS5_SUSPEND#)	O	Suspend control (reserved)
PC2 (VS5_SPKOFF)	O	1: Turn off the speaker
PC3 (VS5_VDCLKEN)	O	1: Video clock enable
PC4 (VS5_VDPD)	O	1: Power down the video controller (in suspend mode)
PC5 (VGADIS)	I	0: Disable VGA controller from PCI
GP0/LED0 (VS5_FLASHRCY)	I	1: Flash ROM recover
GP1/LD1/SUSPA# (VS5_ZZ)	O	Cache sleep
GP2/DDMA_RETRY (VS5_DDMARETRY)	O	DDMA (distributed DMA retry). V3-LS activates this pin to retry V1-LS
GP3/SUPPRESS_RESUME (VS5_COM4_COM3#)	O	Modem I/O address. 1=2E8h, 0=3E8h.
GP4/UNDOCKING (VS5_FLSHVPP)	O	1: Flash ROM Vpp Control
GP5/THRM (SM5_OVTMP)	I	1: over temperature alarm from SMC.
REQ2# (PC3_DKREQ#)	I	0: Dock/undock request, used to tri-state PCI bus before dock/undock.

Table 1- 11 GPIO Port Definition Map

GPIO	I/O	Description
GNT2# (PC5_DKGNT#)	O	0: Dock grant, signal for ready to dock/undock.
WAKE0 (KB5_KBCSMIREQ#)	I	0: Keyboard SMI from KBC and SMC..
WAKE1 (RT5_IRQ8#)	I	0: Wake by RTC alarm
SWITCH (VS5_DOCKIRQ)	I	1: IRQ monitor from docking
RING (VS5_RI#)	I	0: Ring indicator input
EXTACT0 (GR3_VGACT)	I	1: VGA activity from VGA controller ACTIVITY pin.
87C51 (KBC) GPIO Pin Assignment		
LED0 (KB5_KBCSMIREQ#)	O	KBC SMI request
LED1 (KB5_NUMLED#)	O	Keyboard number lock LED control
LED2 (KB5_CAPLED#)	O	Keyboard caps lock LED control
LED3 (KB5_KEYCLICK)	O	Key-click output
P1.0 (KB5_FPAGE1)	O	Force BIOS to high page.
P1.1 (KB5_FPAGE2)	O	FPAGE2 FPAGE1 0 0 F, E0 0 1 F, E1 1 0 F, E2 1 1 reserved
P1.2 (KB5_IDECLKEN)	O	Local bus IDE PCI clock enable
P1.3 (KB5_IITCLKEN)	O	IIT PCI clock enable for video conference
P1.4 (KB5_3MODE)	O	0: 3-mode FDD drive
P1.5 {KB5_CDBEN#)	O	0: Enable CD-ROM buffer 1: Enable FDD buffer
P1.6 (KB5_HDDBEN#)	O	0: Enable HDD buffer
P1.7 (IS5_IRQ12)	O	PS2 mouse IRQ12
P2.0 (KB5_MEMIDA0) P2.1 (KB5_MEMIDA1)	I	Memory ID0 and Memory ID1 for SIMM 1. ID0 ID1 Memory speed 0 0 50nS 0 1 40nS 1 0 70nS 1 1 60nS
P2.2 (KB5_MODE)	I	1: US version (without system power switch) 0: Japan version (with ON/RESUME switch)
P2.3 (KB5_FDD/CD#)	I	1: FDD installed

Table 1- 11 GPIO Port Definition Map

GPIO	I/O	Description
		0: CD-ROM installed
P2.4 (KB5_MDMIDB0) P2.6 (KB5_MDMIDB1)	I	Memory ID0 and Memory ID1 for SIMM 2. ID0 ID1 Memory speed 0 0 50nS 0 1 40nS 1 0 70nS 1 1 60nS
P2.5 (KB5_PSWD)	I	1: Enable password
P2.7 (KB5_OEM)	I	1: Enable Acer logo shown on screen while BIOS POST.
P3.0 (SM5_TXD)	I	UART serial input from SMC.
P3.1 (SM5_RXD)	O	UART serial output to SMC.
P3.2 (KB5_KBDCLK)	I/O	External keyboard clock
87C51 (KBC) GPIO Pin Assignment		
P3.3 (KB5_PTRCLK)	I/O	External PS/2 clock
P3.4 (KB5_KBDDAT)	I/O	External keyboard data
P3.5 (KB5_PTRDAT)	I/O	External PS/2 data
P3.6 (KB5_TOUCHWR#)	O	Touchpad write
P3.7 (KB5_TOUCHRD#)	O	Touchpad read
PCOBF (IS5_IRQ1)	O	IRQ1
AIN0 (KB5_PANID0) AIN1 (KB5_PANID1) AIN2 (KB5_PANID2) AIN3 (KB5_PANID3)	I	Panel ID 0, 1, 2 and 3 ID3 ID2 ID1 ID0 TYPE 0 0 0 0 TFT 0 0 0 1 DSTN
PCDB0~PCDB7 (ISS_SDx)	I	ISA data bus
A0 (IS5_SA2)	I	IO address select: 60h, 64h(for keyboard input buffer)
A1 (IS5_SA1)	I	IO address select: 60h, 64h(for keyboard input buffer)
CSL# (VS5_ROMKBCS#)	I	Keyboard chip select output
RDL# (IS5_IOR#)	I	I/O read
WAL# (IS5_IOW#)	I	I/O write
KSI[0:7] (KB5_KSI[0:7])	I	KB input scan line
KSO[0:15] (KB5_KSO[0:15])	O	KB output scan line
RST(SM5_KBCRST)		Hold "High"
EAL# (KB5_KBCXRAM#)		Hold "High" for internal RAM access
80C51 (KBC) GPIO Pin Assignment (continued)		
LOADREN		Hold 'Low"
ADB[0:7] (KB5_ADB[0:7])	O	External address bus
87C552(SMC) GPIO Pin Assignment		

Table 1- 11 GPIO Port Definition Map

GPIO	I/O	Description
P0.0 (SM5_CHARGON)	O	Charge battery
P0.1 (SM5_MODEN)	O	1: Enable modem buffer
P0.2 (SM5_BMCPWREN#)	O	0: Enable BMCVCC (enable system power)
P0.3 (SM5_P5VRON, SM5_P3VRON)	O	Enable 5V and 3V power
P0.4 (VS5_SUSPEND)	O	Suspend control to V1-LS.
P0.5 (SM5_PWRLED#)	O	Power LED
P0.6 (SM5_BATTLED#)	O	Battery LED
P0.7 (SM5_SMIREQ#)	O	SMI request.
P1.0 (SI5_PNF)	I	1: LPT support FDC through LPT
P1.1 (SM5_1WIRE)	I/O	Dallas 1 wire protocol (communicate with smart battery)
P1.2 (SM5_UNDOCK_REQ#)	I	Undocked request
P1.3 (VS5_CLKEN)	I	Enable clock source (controlled by V1-LS)
P1.4 (SM5_ATN#)	I/O	Communicate with docking station
P1.5 (SM5_RST#)	I/O	Reset docking station
P1.6 (SM5_CLK#)	I/O	I^2C clock through docking station
P1.7 (SM5_DAT#)	I/O	I^2C data through docking station
P2.0 (SM5_IRDAPD)	O	1: Power down SIR
P2.1 (SM5_HDRST#)	O	0: Reset IDE interface.
P2.2 (SM5_BAYSW)	I	0: FDD or CDD module bay is detected
P2.3 (SM5_HDPON)	I	1: Power on the HDD
P2.4 (SM5_MODPON#)	I	1: Power on the modem.
P2.5 (SM5_ROM#)	I	1: Power of the flash ROM(BIOS)
P2.6 (SM5_CDRST#)	I	0: Reset CD-ROM
87C552(SMC) GPIO Pin Assignment (continued)		
P2.7 (SM5_SPPD)	O	1: Power down the serial port buffer
P3.0 (SM5_RXD)	I	UART serial input from KBC
P3.1 (SM5_TXD)	O	UART serial output to KBC
P3.2 (SM5_DOCKSW)	I	1: Docking switch is connected.
P3.3 (SM5_DOCKED)	I	1: Docked completely
P3.4 (SM5_LIDSW)	I	1: Lid switch on (LCD door is closed)
P3.5 (SM5_OVTMP)	O	Over temperature
P3.6 (SM5_CD/FDPON)	O	1: Turn on CD-ROM/FDD power
P3.7 (SM5_ON_RES_SW)	I	1: Docking station power switch is off
P4.0 (SM5_FANON)	O	1: Turn the CPU fan
P4.1 (AUDIO_GPO)	I	1: Power down audio controller, connect to ES1688 GPIO pin.

Table 1- 11 GPIO Port Definition Map

GPIO	I/O	Description
P4.2 (PC3_DKREQ#)	I	Dock request from docking station
P4.3 (SM5_UNDOCK_GNT#)	O	Undock grant to docking station
P4.4 (SM5_ICONT)	I	Charge current control 0: 4mA, normal charge 1: 2mA, over 65° or battery energy is very low
P4.5 (PC3_DKGNT#)	I	Dock grant from V1-LS
P4.6 (SM5_PWRRDY)	O	Power ready, delay about 4ms after notebook power-good signal
P4.7 (SM5_SYSRDY)		SYSRDY
P5.0 (CHARGSP)	I	Adapter type (reserved)
P5.1 (SM5_VBAT_MAIN)	I	Battery voltage
P5.2 (SM5_ACPWRGD)	I	AC source power-good signal
P5.3 (SM5_NBPWRGD)	I	Notebook power-good signal
P5.4 (SM5_THERM_CPU)	I	CPU thermal rating input
P5.5 (SM5_THERM_SYS)	I	System thermal rating input (from charger)
P5.6 (SM5_ACIN_AUX)	I	1: Auxiliary AC adapter is connected (from docking station)
P5.7 (SM5_ACIN_MAIN)	I	1: Main AC adapter is connected
RST (SM5_SMCRST)		
PWM1# (SM5_CONT)	O	LCD contrast
PWM0# (SM5_BRIT)	O	LCD brightness

1.5.6 PCI Devices Assignment

Table 1- 12 PCI Devices Assignment

Device	Assignment
V1-LS	AD10. Chipset Decoded (IDSEL# = 0)
PCI-IDE	AD17(Device 7)
PCI-PCMCIA	AD18(Device 8)
PCI-VGA	AD19(Device 9), INTA#
Video-llT VPIC	AD20(Device A), INTB#
V3-LS	AD21(Device B)
V2-LS	AD22(Device C), INTA#

1.5.7 Power Management

Power Management in this design is aimed toward the conservation of power on the device and system level when the devices or system is not in use. This implies that if any device is detected

as not active for a sustained period of time, the device will be brought to some lower power state as soon as practicable.

With the exception of thermal management, if a device has a demand upon it, full performance and bandwidth will be given to that device for as long as the user demands it. Power management should not cause the user to sacrifice performance or functionality in order to get longer battery life. The longer battery life should be obtained through managing resources not in use.

Pathological cases of measuring CPU speed or trying to periodically check for reaction time of specific peripherals can detect the presence of power management. However, in general, since the device I/O is trapped and the device managed in SMI, the power management of devices should be invisible to the user and the application.

Thermal management is the only overriding concern to the power management architecture. By definition, thermal management only comes into play when the resources of the computer are used in such a way as to accumulate heat and operate many devices at maximum bandwidth to create a thermal problem inside the unit. This thermal problem indicates a danger of damaging components due to excessively high operating temperatures. Hence, in order to maintain a safe operating environment, there may be occasions where we have to sacrifice performance in order to achieve operational safety.

Heuristic power management is designed to operate and adapt to the user while the user is using it. It is the plug and play equivalent for power management. There are no entries in BIOS Setup which are required to be set by the user in order to optimize the computers battery life or operation. The only BIOS Setup entries are for condition information for suspend/resume operations. Normal operations and power management are done automatically. (see chapter 3 BIOS Setup for details).

Since the power management is implemented by linking with APM interface closely, the APM function in Win95 or Win3.1 must be enabled and set to advanced level for optimum power management and the driver that installed in system must be Acer authorized and approved.

1.5.7.1 PMU Timers

There are several devices related timers available on the V1-LS chip. Each timer may have zero or more devices assigned to the timer for the purpose of retriggering the timer.

Table 1- 13 PMU Timers List

Item	Descriptions
Video timer	
Timer value	Heuristic time-out table: 30sec, 1min, 2min, 3min, 4min, 5min, 6min, 7min, 8min, 9min, 10min, 20min, 30min(if AC plugged-in)
System activities and timer retriggers	System activities – The video display (CRT and LCD) is in power saving mode. Timer retriggers – KBC, PS/2 mouse, serial mouse, (if defined in SETUP) will retrigger the timer..

Table 1- 13 PMU Timers List

Item	Descriptions
Detective hardware change	The pin-77 of U24 M2090 (VS5_VDPD) is from L to H.
Modem/parallel/serial timer	
Timer value	Modem/parallel port/COM1/COM2/SIR: 5min, 30min(if AC plugged-in)
System activities and timer retriggers	System activities – Modem controller is in power saving mode. Parallel/serial port pins are in standby mode, serial port clock is stopped (if COM1-4, are not defined as a mouse in BIOS Setup), and parallel port and UART1 decode in the 87336 chip is disabled. Timer retriggers – Modem/parallel port/COM1/COM2/SIR activities
Detective hardware change	Modem: The pin-6 of U3 R6693 (MODVCC) is from H to L. COM1: The pin-25 of U48 MAX211 (SM5_SPPD) is from H to L. COM2/SIR: The pin-1 of Q5 TP0101T (SM5_IRDAPD) is from L to H.
Hard disk timer	
Timer value	First phase heuristic time-out table for entering HDD standby mode: 9sec, 9sec, 20sec, 30sec, 40sec, 50sec, 60sec, 70sec, 80sec, 90sec, 2min, 3min, 4min, 5min, 30min(if AC plugged-in) Second phase fixed timer for entering HDD suspend mode: 9sec
System activities and timer retriggers	System activities – First phase time-out (heuristic) results in hard disk spin down and IDE interface disable. The second time-out (9 sec) results in hard disk power off and IDE controller clock is stopped and its internal HDD buffer disabled. Timer retriggers – The I/O access to 1F0-7, 3F6 will retrigger the timer.
Detective hardware change	1. The pin-89 (CK3_IDECLK) of PCI0643 is tri-stated, IDE controller clock is stopped. 2. The KB5_HDDBEN# signal on pin-1, 13, 37, 25 of 32XL384(U12, IDE interface buffer), and pin-1 of S3384 (U22, IDE interface buffer) are from L to H. HDD buffer is disabled. 3. The pin-41, 42 of CN5 HDD connector (HDDVCC) is from H to L, HDD is powered off.
FDD/CD-ROM timer	
Timer value	The system with internal floppy: 5sec The system with internal CD-ROM[1]: 60sec, 30min(if AC plugged-in)

[1] This parameter is for both internal CD-ROM and external floppy.

Table 1- 13   PMU Timers List

Item	Descriptions
System activities and timer retriggers	System activities – Power off either or both FDD and CD-ROM. Tri-state FDD and CD-ROM interfaces and stop IDE controller clock. Timer retriggers – The I/O access to 3F2, 3F4, 3F5, 3F7, 170-7, 376 will retrigger the timer.
Detective hardware change	1. The pin-89 (CK3_IDECLK) of PCI0643 is tri-stated, IDE controller clock is stopped. 2. The KB5_CDBEN# signal on pin-1, 13 of S3384(UX1 and UX2, IDE interface buffer), and pin-13 of S3384 (U22, IDE interface buffer) are from L to H. CD-ROM buffer is disabled. 3. The pin-30, 31, 32 (CD/FDDVCC) of CN11 FDD/CD connector is from H to L, the FDD/CD-ROM is powered off.

1.5.7.2 Component activities in power saving mode

- **Hard disk**

The hard disk is fully power managed. This means that when the hard disk is not in use, the hard disk is powered off. The following pins are dedicated toward the management of power on the hard disk.

1. IDE controller clock enable [pin-32(KB5_IDECLKEN) of KBC]. Disabled only when both the HDD and the CD-ROM are not in use (timed-out). This pin stops the clock to the IDE controller chip. This chip is static and has no internal power down capabilities.

2. HDD buffer enable [pin-36(KB5_HDDBEN#) of KBC]. When the hard disk is powered off, the buffer disconnects the off-state drive from the still operative controller. The buffer is sequenced to disable the interface before the drive is powered down and to re-enable the interface after the drive is powered up.

3. HDD power enable[pin-42(SM5_HDPON) of SMC]. This pin turns the power on/off for the hard disk only.

4. HDD reset[pin-40(SM5_HDRST#) of SMC]. This pin provides the reset to the drive when the drive is newly powered up. The reset pin is asserted when the drive is first powered up, then the reset is removed after the drive is powered up and before the interface is enabled.

- **CD-ROM**

The CD-ROM and the hard disk are both IDE devices. They share the same controller. The following pins are dedicated toward the management of power on the CD-ROM.

1. IDE controller clock enable[pin-32(KB5_IDECLKEN) of KBC]. This pin is shared with the hard disk. If either the hard disk or the CD-ROM is in use, then the clock enable pin must be enabled.

2. CD-ROM buffer enable[pin-35(KB5_CDBEN#) of KBC]. The CD buffer enable separates the CD-ROM from the IDE controller. This buffer must be disabled before the CD-ROM is turned off. The buffer is re-enabled after the CD-ROM is turned on and brought out of reset.

3. CD-ROM power control[pin-30(SM5_CD/FDPON) of SMC]. The power control pin is used to turn the CD-ROM unit off or on. This pin is shared as a power on/off pin for the floppy disk as well.

If either the internal or external floppy or the CD-ROM is active, then this control pin must be asserted on.

4. CD-ROM Reset[pin-45(SM5_CDRST#) of SMC]. The reset pin is used to assert the hard reset needed for the CD-ROM during power up. The reset pin is asserted before CD-ROM power up and is deasserted after CD-ROM power up and before the buffer is enabled.

- **Floppy**

The floppy has two components involved in the process. The floppy drive and the controller imbedded in the 87336 super I/O chip. The FDC enable/disabled function is controlled by 87336 chip. In power saving mode, there are following condition happened to floppy drive:

1. External pin tri-state. Enabled whenever the floppy is turned off. This control signal is same to CD-ROM buffer enable pin[pin-35(KB5_CDBEN#) of KBC], please see CD-ROM portion for details.

2. PLL disabled. Disabled whenever the floppy and both serial channels are inactive or disabled.

3. FDC power disable. Disables the active decode of the floppy unit. This control signal is same to CD-ROM power control[pin-30(SM5_CD/FDPON) of SMC], please see CD-ROM portion for details.

- **Video**

The video controller has two interfaces for controlling power consumption. The sleep mode is controlled by software and is performed by BIOS calls. The suspend operation is controlled by a VS5_VDPD signal (pin-121 of V1-LS). The video timer is not controlled or retriggered by video activity. Instead, the timer is retriggered by mouse and keyboard activity.

The video chip does have an activity pin (pin-75, ACTIVITY), used to detect activity to the video itself. This pin is used as a speed-up event for the CPU and the determination of software suspend.

- **Serial port**

The serial port is a UART and is contained within the 87366 super I/O chip. The UART operates off of a 14 Mhz clock. The serial port also has a transceiver, a MAX211. Therefore, there are several steps to the power conservation of the serial port as below:

1. Disable the UART1 decode in the 87336 chip.

2. Tri-state the UART1 output pins.

3. Assert the Power Down pin[pin-46(SM5_SPPD) of SMC] on the MAX211 chip.

The MAX211 chip will still pass through the Ring Indicate signal even while in the power down mode(if the Resume On Modem Ring in BIOS Setup is set to enabled). .

4. Disable the 14Mhz clock (If the floppy and the SIR are also disabled).

If the 14Mhz is disabled through the 87336 power down mode, then all serial and floppy functions will fail.

Recovery from power down is the opposite procedure.

- **SIR (UART)**

The SIR port is basically UART. The UART operates off of a 14Mhz clock. The IR port has a DA converter. The UART2 disable control circuit is within the 87336 chip.

1. Tri-state the UART2 output pins.

2. Assert the power down pin [pin-39(SM5_IRDAPD) of SMC] on the DA converter.

3. Disable the 14Mhz clock (If the floppy and the serial port are also disabled).

If the 14Mhz is disabled through the National power down mode, then all serial and floppy functions will fail.

Recovery from power down is the opposite procedure.

- **Parallel port**

Since there are no clock operations on the parallel port, the requirement to power down this area of the 87336 chip are less critical. Also, if the floppy is operated through the parallel port, the parallel port must be enabled to allow operation to continue.

1. Disable the parallel port decode.

- **Modem**

The modem is comprised of several chips and several clocks (independent of the system clocks) for the fax, modem and the voice-over capabilities. There are only two control lines [pin-56(SM5_MODEN) and pin-43(SM5_MODPON#) of SMC] and one software interface for the power controls on the modem.

The modem chip set cannot be actively power managed. If the modem is enabled, through BIOS Setup, then the S24 register is used to control the power consumed by the modem. If BIOS Setup is set to disable the modem, then the modem enable and modem power pins are used to remove the modem from the circuit entirely.

Modem Enable. A master enable pin[pin-56(SM5_MODEN) of SMC] can be asserted to stop the decode and therefore the selects of the modem chip. This line is used exclusively in cases of modem power off conditions.

Modem power enable. This pin[pin-43(SM5_MODPON#) of SMC] will control the power to all of the modem chips. Once powered down, the modem chip set has no means of recovery except through full software initialization.

- **Audio**

The audio chip has an internal power down mode available. This is done through a self timer. However, this self timer has two possible configurations. When the self timer expires, the digital section will power down and conserve power. There is an option to power down the analog section as well. If the analog section is power down with the timer, then CD music played directly from the CD to the audio port will be unavailable. Similarly, any playback through the line-in will be ignored.

- **CPU**

The STPCLK# signal. Assertion of the STPCLK# [pin-20(STPCLK#/SUSP#) of V1-LS] signal will stop the clock to the core of the CPU. This line can be modulated to allow the CPU to achieve a simulated lower clock rate. The STPCLK# signal only affects the CPU core. The internal cache and the bus handshake are still active when the STPCLK# signal is asserted.

The CPU clock. The clock to the CPU can be physically stopped. The chip is static, so the current state is retained. During a clock stop state, the CPU is stopped and the internal cache and external bus signals are inoperative. Therefore, any bus master or DMA activity is halted as well.

CPU thermal alarm. Thermal alarm is signaled by the assertion of the one control pin [pin-126(SM5_OVTMP) of V1-LS], will trigger a lower speed operation through clock throttling while the CPU temperature is higher than 80°C, shut down the system while higher than 95°C. The system returned to normal condition while the CPU temperature is lower to 75°C.

- **System**

The system can also be put into a low power state. However, this state can only be performed after the individually power managed components have achieved their low power state. The state where the system is put into lower power mode is termed static suspend (suspend-to-memory).

System thermal alarm. System thermal rating is obtained by the a thermal sensor aside charger and signaled by the pin-64(SM5_THERM_SYS) of SMC. Full charge to battery is only available when the system temperature is less than 56°C while trickle charge higher than 58°C. System shutdown will be automatically executed while temperature is higher than 85°C.

1.5.7.3 Suspend

There are two forms of suspend and resume on the notebook, static suspend(suspend-to-memory) and zero-volt suspend(suspend-to-disk). Zero-volt suspend is, as the name implies, an OFF condition. The entire computer state is saved to a disk file and the computer is turned off. In static suspend, all components are placed into an idle state and the clocks are stopped to the entire machine, except for the 32 kHz clock for memory refresh.

In either case, all separate components in the system are put into their lowest power state **at the start** of either suspend process.

1. **Devices turned off.** The HDD(except for suspend-to-disk since the file goes there), CD-ROM, floppy are turned off at the start of any suspend.

2. **Devices brought to a low power state.** The modem, audio, serial port transceiver (MAX213), SIR, keyboard controller, PCMCIA controller chip will be put into a low power state instantly through a pin asserting or prematurely expiring the device timer.

3. **Devices zero-clocked.** Since the remainder of the devices (video, CPU, IDE controller, ISA bus, 87336's devices (serial and floppy)) are, by design, static devices, their lowest power states are achieved by removing the clock to the device.

The very act of going into a suspend-to-memory means that the enable pin to the clock generator chip is deasserted, removing all but the 32 kHz signal from the board. This excludes, however, the clocks dedicated to the internal modem. They will remained powered and oscillating.

For suspend-to-disk, all devices are read, saved to local memory and the local memory, video memory are saved to a disk file which is created by SLEEP MANAGER utility. The machine is then commanded to an off state.

- **Resume events for zero-volt suspend(suspend-to-disk)**

  The only resume event for zero-volt suspend is the raising of the lid of the computer. This electronically enables the power to the rest of the machine.

- **Resume events for static suspend(suspend-to-memory)**

  1. **Resume on modem ring.** This is set in BIOS Setup in the power management section. Enabling of this field to any ring count will disable the suspend to function, except for battery very low.
  2. **Resume on schedule.** In BIOS Setup, this time field can be enabled then set to any value. It is possible to set it for a date and time in the past. In this case, the unit will resume at the next occurrence of the specified time, date ignorant. If a proper future date is specified, then the resume will only happen long enough to evaluate the date and the machine will re-suspend. After a successful resume has taken place, the resume on schedule field will automatically disable. . Enabling of this field will disable the suspend-to-disk function, except for battery very low. The auto-disable of resume on schedule

still allows the unit to suspend to disk at the next occurrence of a suspend condition with the lid closed.

3. **Lid switch.** If the suspend-to-disk option is used, then the lid switch will turn the unit on, reboot and then resume to the application at the end of POST. If the suspend-to-memory option is in place, or a suspend-to-disk block is present, then the lid switch opening will resume the machine.

4. **Keystroke.** Any key use on the internal keyboard will wake up the system from static suspend. In addition, a keystroke from an external keyboard on the primary PS/2 port will also wake the system up. Mouse motion from any source will not wake the system up.

5. **Battery very low.** The SMC will wake the SMI if the battery reaches a very low condition during static suspend.

1.5.8 CPU

Table 1- 14 CPU Specifications

Item	Specification
CPU Type	P54CSLM-120/-133/-150
Package	TCP
Switchable processor speed	Yes
Minimum working speed	0MHz
CPU voltage	3.3V/3.1V/2.9V/2.7V/2.5V

1.5.9 BIOS

Table 1- 15 BIOS Specifications

Item	Specification
BIOS programming vendor	Acer
BIOS version	V2.0
BIOS ROM type	Intel 28F002, Flash ROM with boot block protection
BIOS ROM size	256KB
BIOS ROM package type	40-pin TSOP
Same BIOS for STN or TFT LCD type	Yes
Boot from CD-ROM feature	Yes
Support protocol	PCI V2.1, APM V1.1, E-IDE and PnP(ESCD format) V1.0a
BIOS flash security protection	Provide boot-block protection[1] feature.
Unlock BIOS feature	If user changes the BIOS Setup setting and causes the system cannot boot, press before system turns-on till POST completed, then system will load BIOS Setup the default

[1] Boot-block is an area inside of BIOS with the program for system boot. Avoid this area to be modified while BIOS flash, then system still can boot even the BIOS flash process is not successful.

	settings.

1.5.10 System Memory

Table 1- 16 System Memory Specifications

Item	Specification
SIMM data bus width	64-bit
SIMM package	144-pin, Small Outline Dual-In-line-Memory-Module (soDIMM)
SIMM size	8MB, 16MB or 32MB
SIMM speed	60ns
SIMM voltage	3.3V
EDO can be mixed with FPS	Yes

1.5.10.1 SIMM memory combination list

Table 1- 17 SIMM memory combination list

Slot #1	Slot #2	Total
8MB	0MB	8MB
0MB	8MB	8MB
0MB	16MB	16MB
8MB	8MB	16MB
16MB	0MB	16MB
8MB	16MB	24MB
16MB	8MB	24MB
0MB	32MB	32MB
16MB	16MB	32MB
32MB	0MB	32MB
8MB	32MB	40MB
32MB	8MB	40MB
32MB	16MB	48MB
16MB	32MB	48MB
32MB	32MB	64MB

1.5.11 Cache Memory

Table 1- 18 Cache Memory Specifications

Item	Specification
First level cache	
Cache enabled/disabled control	By BIOS Setup
Second level cache	
SRAM size	256KB
SRAM type	Pipe-line burst SRAM
SRAM configuration	32K*32 x 2pcs
SRAM package	SQFP
Voltage	3.3V
Cache enabled/disabled control	By BIOS Setup
Cache scheme control	By BIOS Setup (Write-back / Write through)

1.5.12 Video Memory

Table 1- 19 Video Memory Specification

Item	Specification
Memory size	1.1MB
Memory location	Inside of graphic controller NMG2090

1.5.13 Video Display Modes

Table 1- 20 Video Display Specification

Item	Specification
Chip vendor	NeoMagic
Chip name	NMG2090
Chip voltage	3.3 Volts
ZV port support (Y/N)	No
Graph interface (ISA/VESA/PCI)	PCI bus
Max. resolution (LCD)	800x600 (64K colors)
Max. resolution (Ext. CRT)	1024x768 (256 colors)

1.5.13.1 External CRT Resolution Modes

Table 1- 21 External CRT Resolution Modes

Resolution x Color on Ext. CRT	CRT Refresh Rate		Simultaneous on TFT LCD	Simultaneous on STN LCD
	CRT only	Simultaneous	SVGA	SVGA
640x480x256	60,75,85	60	Y	Y
640x480x64K	60,75,85	60	Y	Y
640x480x16M	60,75,85	60	Y	Y
800x600x256	60,75,85	60	Y	Y
800x600x64K	60,75,85	60	Y	Y
1024x768x256	60	60	Y	Y

1.5.13.2 LCD Resolution Modes

Table 1- 22 LCD Resolution Modes

Resolution x color on LCD only	SVGA TFT LCD	SVGA STN LCD
640x480x256	Y	Y
640x480x64K	Y	Y
640x480x16M	Y	Y
800x600x256	Y	Y
800x600x64K	Y	Y
1024x768x256	Y	Y

1.5.14 Audio

Table 1- 23 Audio Specifications

Item	Specification
Chipset	ES1688W
Audio onboard or optional	Built-in
Mono or stereo	stereo
Resolution	16-bit
Compatibility	Sound Blaster PRO V3.01
Music synthesizer	20-voice, 72 operator, FM music synthesizer
Mixed sound sources	Voice, Synthesizer, Line-in, Microphone, CD
Voice channel	8-/16-bit, mono/stereo

Table 1- 23 Audio Specifications

Item	Specification
Sampling rate	44.1 kHz
MPU[1]-401 UART support	Yes
Internal microphone	Yes
Internal speaker / quantity	Yes / 2pcs
Internal speaker enabled/disabled function	By BIOS Setup
Microphone jack	Yes, left side
Headphone jack	Yes, left side
Base address (by BIOS Setup)	220h / 230h / 240h / 250h
MPU address (by BIOS Setup)	300h / 310h / 320h / 330h
IRQ setting (auto-allocation)	IRQ10/ 9/ 7/ 5
DMA channel (auto-allocation)	DRQ0/ 1/ 3

1.5.15 Modem

Table 1- 24 Modem Specifications

Item	Specification
Chipset	RCV288Aci/SVD Modem Chipset
Fax modem data baud rate (bps)	28800
Data modem data baud rate (bps)	14400
Support modem protocol	V.34 data modem, V.17 fax modem, voice/audio mode, and digital simultaneous voice and data (DSVD) operation over a dial-up telephone line
Modem connector type	RJ11
Modem connector location	Rear side

1.5.16 PCMCIA

Table 1- 25 PCMCIA Specifications

Item	Specification
Chipset	Cirrus Logic CL-PD6730
Supported card type	Type-II / Type-III
Number of slots	Two Type-II or one Type-III
Access location	Left side
ZV port support	No

[1] MPU-401 is a Roland MIDI standard that most of the game software used for audio use.

1.5.17 Parallel Port

Table 1- 26 Parallel Port Specifications

Item	Specification
Number of parallel ports	1
ECP/EPP support	Yes (by BIOS Setup)
ECP DMA channel (by BIOS Setup)	DRQ1 or DRQ3
Connector type	25-pin D-type
Connector location	Rear side
Selectable parallel port (by BIOS Setup)	Parallel 1 (378h, IRQ7) or Parallel 2 (3BCh, IRQ7) or Parallel 3 (278h, IRQ5) or Disabled

1.5.18 Serial Port

Table 1- 27 Serial Port Specifications

Item	Specification
Number of serial ports	1
16550 UART support	Yes
Connector type	9-pin D-type
Connector location	Rear side
Selectable serial port (by BIOS Setup)	Serial 1 (3F8h, IRQ4) or Serial 2 (2F8h, IRQ3) or Serial 3 (3E8h, IRQ4) or Serial 4 (2E8h, IRQ3) or Disabled

1.5.19 Touchpad

Table 1- 28 Touchpad Specifications

Item	Specification
Vendor & model name	Synaptics TM1002SC
Power supply voltage	5V
Location	Palm-rest center
Internal & external pointing device work simultaneously	No
External pointing device (serial or PS/2 mouse) hot plug	Yes, (if it is enabled in BIOS Setup already)
X/Y position resolution	500 points/inch (200
Interface	PS/2 (compatible with Microsoft mouse driver)

1.5.20 SIR

Table 1- 29 SIR Specifications

Item	Specification
Vendor & model name	TEMIC TFDS3000
Input power supply voltage	5 V
Transfer data rate	115.2 Kbit/s
Transfer distance	100cm
Compatible standard	IrDA (Infrared Data Association)
Output data signal voltage level Active Non-active	 0.5 Vcc-0.5
Angle of operation	±15°
Number of IrDA ports	1
16550 UART support	Yes
SIR location	Rear side
Selectable serial port (by BIOS Setup)	2F8h, IRQ3 Disabled

1.5.21 LCD

Table 1- 30 LCD Specifications

Item	Specification	Specification	Specification
Vendor & Model Name	HITACHI LMG9930ZWCC	HITACHI TX30D01VC1CAA	IBM ITSV50D
Mechanical Specifications			
Diagonal LCD display area	11.3”	11.8”	12.1”
Display technology	STN	TFT	TFT
Resolution	SVGA (800x600)	SVGA (800x600)	SVGA (800x600)
Supported colors	--	262,144 colors	262,144 colors
Optical Specification			
Contrast ratio	30(typ.)	80 (typ.)	100 (typ.)
Brightness (cd/m^2)	70 (typ.)	70 (typ.)	70 (typ.)
Brightness control	keyboard hotkey	keyboard hotkey	keyboard hotkey
Contrast control	keyboard hotkey	none	none
Electrical Specification			
Supply voltage for LCD display	3.3 (typ.)	3.3 (typ.)	3.3 (typ.)
Supply voltage for LCD backlight (Vrms)	590 (typ.)	2000 (max.)	1500 (typ.)

1.5.22 CD-ROM

Table 1- 31 CD-ROM Specifications

Item	Specification
Vendor & model name	Toshiba XM1402B
Internal CD-ROM/FDD hot-swappable	No
BIOS auto-detect CD-ROM existence	Yes
BIOS support boot from CD drive feature	Yes
Performance specification	
Speed	900KB/sec(6X speed)
Access time	190ms
Buffer memory	128kbyte
Interface	Enhanced IDE (ATAPI) compatible (communicate with system via system E-IDE channel 2)
Applicable disc format	Red-Book, Yellow-Book, CD-ROM XA, CD-I, Bridge (Photo-CD, Video CD), CD-I, CD-I Ready, CD-G and Multi-session (Photo-CD, CD EXTRA)
Loading mechanism	Drawer type, manual load/release
Power Requirement	
Power supply voltage (V)	5

1.5.23 Diskette Drive

Table 1- 32 Diskette Drive Specifications

Item	Specification		
Vendor & model name	Mitsumi D353F2		
Internal FDD/CD-ROM hot-swappable	No		
BIOS auto-detect external FDD existence	Yes		
External FDD hot-swappable	Yes		
Floppy Disk Specifications			
Media recognition	2DD (720K)	2HD (1.2M, 3-mode)	2HD (1.44M)
Sectors / track	9	15	18
Tracks	80	80	80
Data transfer rate (Kbits/s)	250 300	500	500
Rotational speed (RPM)	300 360	360	300
Read/write heads	2		
Encoding method	MFM		
Power Requirement			
Input Voltage	+5V ± 10%		

1.5.24 Hard Disk Drive

Table 1- 33 Hard Disk Drive Specifications

Item	Specification	
Vendor & Model Name	IBM DMCA-21440	IBM DCRA 22160
Drive Format		
Capacity (MB)	1440	2160
Bytes per sector	512	512
Logical heads	16	16
Logical sectors	63	63
Logical cylinders	2800	4200
Physical read/write heads	4	6
Disks	2	3
Spindle speed (RPM)	4009	4900
Performance Specifications		
Buffer size (KB)	96	96
Interface	ATA-2	ATA-2
Data transfer rate (disk-buffer, Mbytes/s)	4.9 ~ 7.7	6.1 ~ 9.3
Data transfer rate (host-buffer, Mbytes/s)	16.6 (max., PIO mode 4)	16.6 (max., PIO mode 4)
DC Power Requirements		
Voltage tolerance (V)	5 ± 5%	5 ± 5%

1.5.25 Keyboard

Table 1- 34 Keyboard Specifications

Item	Specification		
Vendor & Model Name	SMK KAS1901-0111R (English)	SMK KAS1901-0132R (Germany)	SMK KAS1901-0151R (Japanese)
Total number of keypads	84 keys	85 keys	88 keys
Windows95 keys	Yes, (Logo key / Application key):	Yes, (Logo key / Application key):	Yes, (Logo key / Application key):
External PS/2 keyboard hot plug	Yes		
Internal & external keyboard work simultaneously	Yes		
Keyboard automatic tilt feature	Yes The keyboard has the option of automatically tilting to a six-degree angle whenever you open the lid. This feature is set by an keyboard automatic tilt latch on the rear side of the system unit.		

1.5.26 Battery

Table 1- 35 Battery Specifications

Item	Specification
Vendor & Model Name	Sony LIP617LACP
Battery Gauge	Yes
Battery type	Li-Ion
Cell capacity	900mAH
Cell voltage	3.6V
Number of battery cell	6-Cell
Package configuration	3 serial, 2 parallel
Package voltage	10.8V
Package capacity	58.3WH
Second battery	No

1.5.27 DC-DC Converter

DC-DC converter generates multiple DC voltage level for whole system unit use, and offer charge current to battery.

Table 1- 36 DC-DC Converter Specifications

Item	Specification				
Vendor & Model Name	Ambit T62.036.C.00				
Input voltage (Vdc)	7 - 19				
Short circuit protection	The DC/DC converter shall be capable of withstanding a continuous short-circuit to any output without damage or over stress to the component, traces and cover material under the DC input 7~19 V from AC adapter or 18V from battery. It shall operate in shut down mode for the shorting of any de output pins.				
Output rating	**BMCVCC (5V)**	**P5VR (3.3V)**	**P3VR (3.3V)**	**P12VR (+12V)**	**CHRGOUT (0 ~ 3.5A)**
Load range (w/load, A)	0 ~ 0.5	0 ~ 2.5	0 ~ 3	0 ~ 0.5	0 ~ 4
Load range (w/load, V)	-	-	-	-	0 ~ 13.5
Voltage ripple + noise (max., mV)	100	100	100	100	400

1.5.28 DC-AC Inverter

DC-AC inverter is used to generate very high AC voltage, then supply to LCD CCFT backlight use. The DC-AC inverter area should be void to touch while the system unit is turned on.

Table 1- 37 DC-AC Inverter Specifications

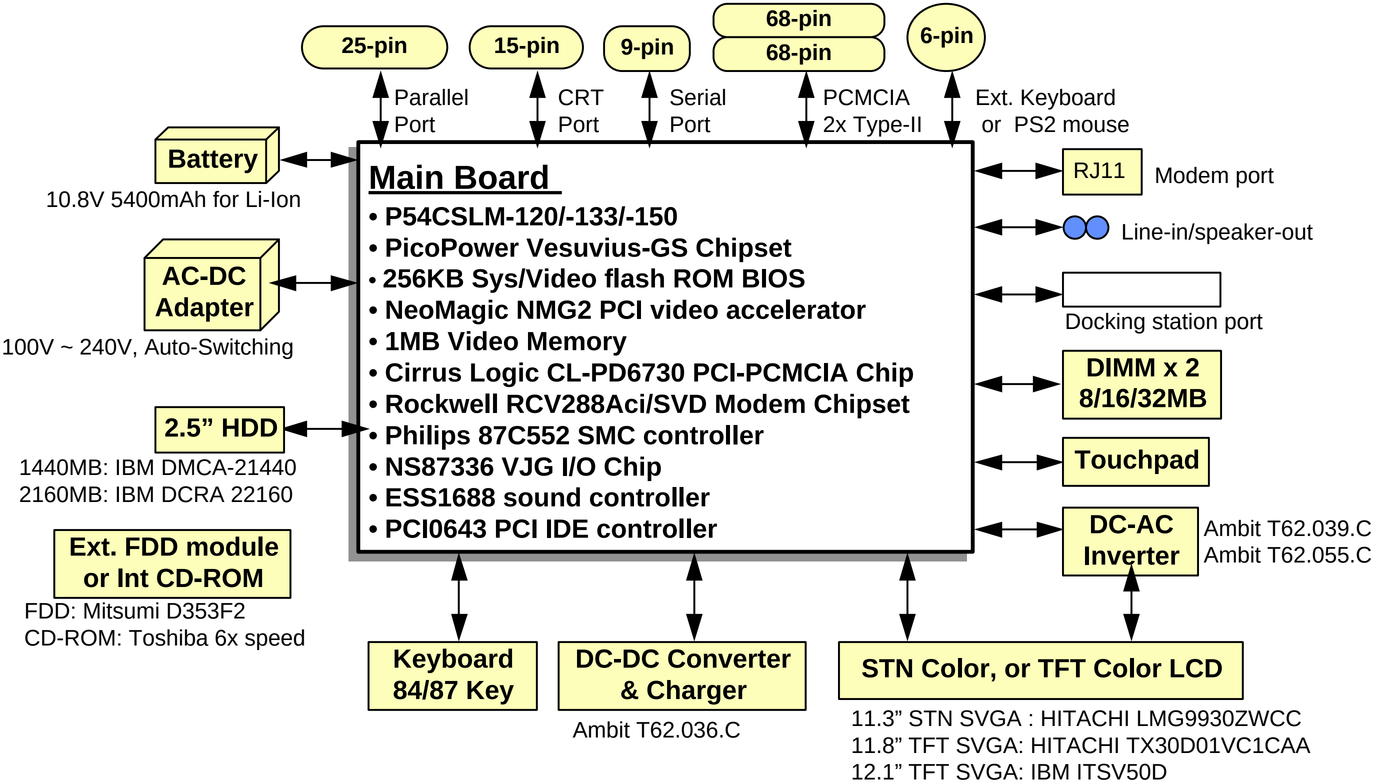
Item	Specification	
Vendor & Model Name	Ambit T62-039.C.00	Ambit T62-055.C.00
Used LCD type	HITACHI LMG9930ZWCC HITACHI TX30D01VC1CAA	IBM ITSV50D
Input voltage (V)	7 ~ 19	7 ~ 19
Output voltage (Vrms, with load)	450 ~ 550	650 (typ.)
Output current (mArms, with load)	1.5 ~ 4.5	2 ~ 5

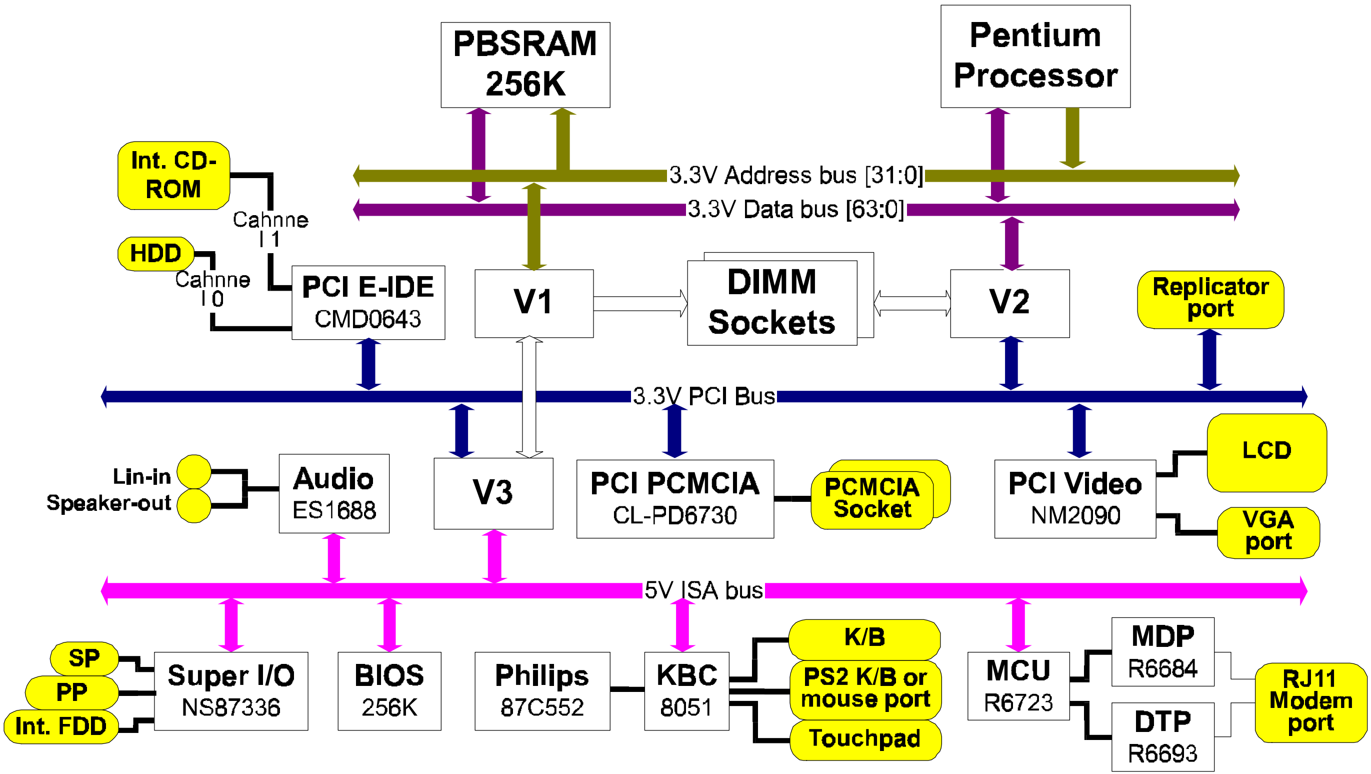
1.5.29 AC Adapter

Table 1- 38 AC Adapter Specifications

Item	Specification
Vendor & Model Name	EOS, ZVC70NS-18.5
Input Requirements	
Nominal voltages (Vrms)	90 - 264
Nominal frequency (Hz)	47 - 63
Inrush current (A)	30 (@264Vac)
Efficiency	86% (min., @18V,3.6A output and 230Vac input)
Output Ratings	
Output power (W)	65
Output voltage (V)	+18
Noise + Ripple (mV)	200
Load (A)	0 (min.) 3.6 (max.)
Dynamic Output Characteristics	
Turn-on delay time	1 sec (max.)
Hold up time	3 ms (min., @ 115 Vac input)
Short circuit protection	Output can be shorted without damage
Dielectric Withstand Voltage	
Primary to secondary	3000 Vac for 1 minutes
Leakage current	250µA (max)
Regulatory Requirements	
1. CISPR 55022 and CISPR55014, class B (@230Vac and 115Vac) requirements. [Scandinavia] 2. FCC 47 CFR Part15, class B (115Vac) with 6db of margin. [USA]	

1.6.1 System Functional Block Diagram




PBSRAM 256K
Pentium Processor
Int. CD-ROM
Cahnne l 1
HDD
Cahnne l 0
3.3V Address bus [31:0]
3.3V Data bus [63:0]
PCI E-IDE CMD0643
V1
DIMM Sockets
V2
Replicator port
3.3V PCI Bus
Lin-in
Speaker-out
Audio ES1688
V3
PCI PCMCIA CL-PD6730
PCMCIA Socket
PCI Video NM2090
LCD
VGA port
5V ISA bus
SP
PP
Int. FDD
Super I/O NS87336
BIOS 256K
Philips 87C552
KBC 8051
K/B
PS2 K/B or mouse port
Touchpad
MCU R6723
MDP R6684
DTP R6693
RJ11 Modem port

1.7. Environmental Requirements

Table 1- 39 Environmental Requirements

Item	Specification
Temperature	
Operating (ºC)	+5 ~ +35
Non-operating(ºC)	-20 ~ +60
Humidity	
Operating (non-condensing)	20% ~ 80%
Non-operating (non-condensing)	20% ~ 90%
Operating Vibration (unpacked)	
Operating	5 - 25.6Hz, 0.38mm; 25.6 - 250Hz, 0.5G
Sweep rate	> 1 minute / octave
Number of test cycles	2 / axis (X,Y,Z)
Non-operating Vibration (unpacked)	
Non-operating	5 - 27.1Hz, 0.6G; 27.1 - 50Hz, 0.41mm
Sweep rate	> 2 minutes / octave
Number of text cycles	4 / axis (X,Y,Z)
Shock	
Operating	5G peak, 11±1ms, half-sine
Non-operating (unpacked)	40G peak, 11±1ms, half-sine
Non-operating (packed)	50G peak, 11±1ms, half-sine
Altitude	
Operating	10,000 feet
Non-operating	40,000 feet
ESD	
Air discharge	10kV (no error) 12.5kV (no restart error) 15kV (no damage)
Contact discharge	6kV (no error) 7kV (no restart error) 8kV (no damage)

1.8. Mechanical Specifications

Table 1- 40 Mechanical Specifications

Item	Specification
Weight (includes battery) with FDD module with CD-ROM module	 3.4 kg. (7.4 lbs.) 3.5 kg. (7.7 lbs.)
Dimensions round contour main footprint	 297~313mm x 230~240mm x 48~53mm 11.7” x 9.1” x 2”

Major Component Introduction

This chapter discusses the major components.

2.1 Major Component List

Table 2-1 Major Chips List

Component	Vendor	Description
Vesuvius-LS Chipset PT86C521(V1-LS) PT86C522(V2-LS) PT86C523(V3-LS)	Pico Power	 System Controller Data Path Controller PCI to ISA Controller
NMG2090	NeoMagic	Video/LCD controller
RCV288Aci/SVD Modem Chipset R6723-12 R6684-17 R6693-14	Rockwell	 MCU (Microcomputer) Chip MDP (Modem Data Pump) Chip DTP (DigiTalk Processor) Chip
ES1688W	Creative Tech.	Sound controller
87C552	Philips	Single-chip 8-bit controller for SMC (System Management Controller)
NS87336VLJ	NS (National Semiconductor)	Super I/O controller
CL-PD6730	Cirrus Logic	PCI PCMCIA controller
PCI0643	CMD Tech.	PCI local bus E-IDE controller
T62.036.C.00	Ambit	DC-DC Converter
T62.039.C.00 T62.055.C.00	Ambit	DC-AC Inverter

2.2 PicoPower Vesuvius-LS Chipset

The VESUVIUS platform is a high-performance, highly integrated system solution for IBM-AT-compatible computers offering universal support for Intel's 3.3-V Pentium processor and comparable 64-bit processors from AMD and Cyrix. Based on a PCI Local Bus native architecture, it offers a superior, power-efficient solution for both desktop and portable computers.

VESUVIUS is a native PCI system controller solution for the 3.3-V 75-, 90-MHz and 100- MHz Pentium processors from Intel. It connects the Pentium processor bus to the industry-standard PCI Local Bus and provides a bridge between the PCI and ISA busses to support popular ISA bus peripherals.

The VESUVIUS platform supports a full product line by offering different options to implement the second level cache and the DPAM subsystems. The VESUVIUS system solution also supports a cacheless system configuration by providing a sophisticated DRAM controller that supports leading edge DRAM technology.

The V1-LS and V2-LS provide a native PCI interface to the Pentium processor bus along with a 64-bit L2 cache controller and a 64- and 32-bit mixed mode DRAM controller. V3-LS provides a bridge between the PCI and the ISA bus. The PCI Local Bus architecture automatically provides Plug-and-Play functionality for PCI peripheral devices.

Implemented in 0.6µm CMOS technology, this platform supports a full range of the Pentium processor bus frequencies from 50- to 66-MHz. Synchronous between the CPU and the PCI bus enables superior performance on 25- and 33-MHz PCI bus.

VESUVIUS makes best-of-class performance possible by virtue of its rich feature set, advanced architecture, and incomparable power management. The VESUVIUS system solution offers the highest level of power and thermal management for the Pentium processor systems, using PicoPower's patented Power on Demand technology that includes active and passive power management and heat regulation.

An innovative programming model simplifies the BIOS development task without compromising any power management features. The power management control implemented in VESUVIUS goes beyond the standard EnergyStar requirements. It offers an excellent time-to-market system solution for Pentium processor-class portable systems. The VESUVIUS portable system solution provides all the hooks required to support PCI and ISA hot and warm docking, enabling a full-featured docking station design.

The V1-LS chip integrates the CPU bus to the PCI bus interface controller/arbiter, an L2 cache controller. a DRAM controller and the power management controller. It takes full advantage of the Pentium processor performance by supporting CPU bus frequencies up to 66-MHz. By implementing both toggle and linear burst mechanism, the V1-LS is armed with the support for Pentium-class processors from multiple vendors.

The integrated, 64-bit, direct-mapped L2 cache controller supports synchronous SRAM, external TAG compare (for TAG RAMs) and both buffered write-through and write-back cache update schemes for highest performance. The DRAM controller implements the logic required to use advanced, high speed DRAMs that reduce the performance overhead of the L2 cache miss cycles. The V1-LS has the control logic for write buffers in V2-LS to achieve 2-1-1-1 burst writes. It implements a synchronous interface between the CPU and PCI buses to exploit the maximum potential of PCI bandwidth. The V1-LS supports 64-bit, two-way-set associative write-back cache with Sony's Sonyc-2WP.

The V1-LS supports power management features like SMM, SMI, Stop Clock, and AutoHalt. It also features a thermal control mechanism that uses CPU clock throttling to efficiently control the power consumption and heat dissipation associated with the processor.

The V2-LS data path controller provides a 64-bit data path between the CPU and the main memory; a 32-bit data path between the CPU bus and the PCI local bus, and a 32-bit data path between the PCI local bus and the main memory. The eight-level deep, 64-bit write-buffers implemented in the V2-LS device are quad-word-wide and substantially improve the CPU-to-memory and the CPU-to-PCI write performance. The VESUVIUS architecture offers a cost-efficient interface between the V2-LS and V1-LS devices, enabling a single chip implementation of the entire data path control.

The V3-LS chip completes the VESUVIUS solution for desktop/portable systems. Its primary function is to act as a bridge between the PCI and the ISA bus. The V3-Gs provides interface between the PCI local bus and the industry-standard ISA expansion bus. It has the logic to support master and slave cycles on both PCI and ISA buses. The V3-LS integrates most I/O functions such as DMA controllers, interrupt controllers, programmable interval timer, memory mapper, and hidden ISA refresh controller found in ISA-based personal computers.

The V3-LS isolates the PCI bus and the ISA bus by providing the data buffers and buffer control logic. It has a special serial interface with V1-LS to support power management features including ISA bus device activity detection and other PicoPower-proprietary features. Additionally, the V3-LS supports proven ISA hot/warm docking by appropriately tri-stating the ISA bus. Available in a 176-pin TQFP package, the V3-LS chip also contains a highly integrated peripheral controller.

Features

- Optimized three-chip PCI system controller solution for Intel’s Pentium™ processors
- Universal support for AMD's K5 and Cyrix's M1 64-bit processors
- Supports all 3.0v processors with speeds up to 100 MHz
  - Supports processor bus frequencies of 50-, 60-, and 66-MHz
- Native PCI Local Bus architecture with direct connection to the Pentium processor bus
- Vesuvius-LS: Ideally suited for entry-level to midrange portable systems and energy-efficient desktop computers
- Supports L1 (level-1) write-back or write-through cache protocols
- Space-efficient, two 208-pin and one 176-pin TQFP packages
  - 0.6-µm CMOS technology
- 100% IBM-AT compatible
- PicoPower's exclusive Power on Demand III
- Best-of-class power and thermal management
  - Employs PicoPower's patented Power on Demand technologies to achieve superior power efficiency
  - Active power management cuts power consumption even when the system is in use

- Passive power management cuts power consumption when the system is idle
    - Supports SMM (system management mode), SMI (system management interrupt), Stop Clock, and AutoHalt
    - Flexible hybrid voltage implementation
    - Optional thermal control with thermal clock throttling
    - User-programmable power setting (10 percent granularity)
    - Deep Sleep and Suspend-to-Disk modes
    - Supports wake control, interrupt-as-wake-source, and ring-output-as-wake-source
    - External activity detection
    - Status indicator
    - Supports 3.3-V processor bus, 3.3V/5-V PCI bus, 5-V ISA bus, 3.3V L2 cache controller, and 3.3V/5-V DRAM subsystem

- Supports both toggle and linear burst sequences
- Supports CPU address pipelining and burst read/write
- Supports eight-level write-buffer for DRAM and PCI cycles
- Integrated 64-bit write-through and write-back Level 2 (L2) cache controller
    - Direct-mapped
    - Supports cache size of 256 Kbytes to 1 Mbyte with 32byte line size
    - Supports synchronous or asynchronous 3.3-V SRAM
    - Internal and external TAG compare
    - Supports 2-1-1-1 burst read and write with 10 ns synchronous (15 ns cycle time) SRAM and with 8 ns TAG RAM at 66-MHz and O1-1-1 with 10 ns synchronous SRAM and internal TAG compare at 66-MHz
    - One less wait-state for read lead-off cycle with pipelining
    - Supports S2-2-2 burst write with 17 ns asynchronous SRAM and 15 ns TAG SRAM with internal TAG compare at 66-MHz
    - Intelligent L2 cache power management, including stop dock for synchronous SRAMs, and TAG chip select for TAGRAM
- Supports 64-bit 2-way set associative writeback cache with Sony's Sonyc-2WP
- Built-in DRAM controller
    - Mixable 64- or 32-bit DRAM bank support
    - 3.3-V and 5-V DRAM support
    - Up to 256 Mbytes of system memory
    - Four banks of 64-bit DRAM or eight banks of 32-bit DRAM
    - Supports 256 Kbit, 512 Kbit, 1 Mbit, 2 Mbit, 4 Mbits, and 16 Mbit DRAM
    - Support for symmetric and asymmetric DRAM

- Supports mixed FPM (fast page mode) and EDO (extended data output) DRAM
- Slow/self refresh support, including hidden, staggered, CAS-before-RAS refresh or RAS only refresh
- Dedicated DRAM memory address and data busses
- 5-2-2-2 burst read cycles with 60-ns EDO DRAM at 66-MHz
- 6-3-3-3 page-hit and 10-3-3-3 page-miss burst-read cycles with 60-ns standard DRAM at 66-MHz
- Two less wait-states in the lead-off cycle for pipeline access
- Write-buffers for CPU generated DRAM cycles
- Supports read reordering
- Support for ROM shadowing
- SMM RAM size from 32 Kbyte to 128 Kbyte. Easy SMI code copying to SMM RAM in normal memory mode

- PCI Local Bus native architecture
  - Supports 32-bit PCI Local Bus
  - Supports both 3.3-V and 5-V PCI
  - Provides synchronous interface between the CPU bus and the PCI bus
  - PCI Local Bus revision 2.01 compliant
  - Supports Mobile PCI specification
  - Supports PCI burst cycles
  - Maximum 5 PCI masters and 4 PCI slots
  - Integrated PCI bus arbiter with rotating priority
  - PCI parity and system error support
  - PCI-to-ISA memory post-write - PCI interrupt steering
  - Intelligent power management through clock scaling
- Docking station support

- PCI to ISA bridge
  - 33 MHz operation on the PCI bus
  - Fully supports the ISA bus
  - Master/slave interface for the PCI and the ISA bus
  - PCI-to-ISA and ISA-to-PCI bus cycle translations
- Hidden AT bus refresh
- Quiet bus
- Supports PC parity and system error
- 8-bit BIOS ROM, FLASH EPROM support
- Generates chip select for external KBC (keyboard controller)
- Coprocessor interface
- Highly integrated peripheral controller
  - Two 82C57 DMA controllers
  - One 82C54 programmable interval timer
  - Two 82C59A interrupt controllers
  - One 74LS612 memory mapper
  - Hidden ISA refresh controller
  - PCI interface controller
  - ISA interface controller
  - Power management interface

Architecture Block Diagram

The following is the architectural block diagram of the PicoPower Vesuvius chipset with respect to its implementation in this notebook computer.

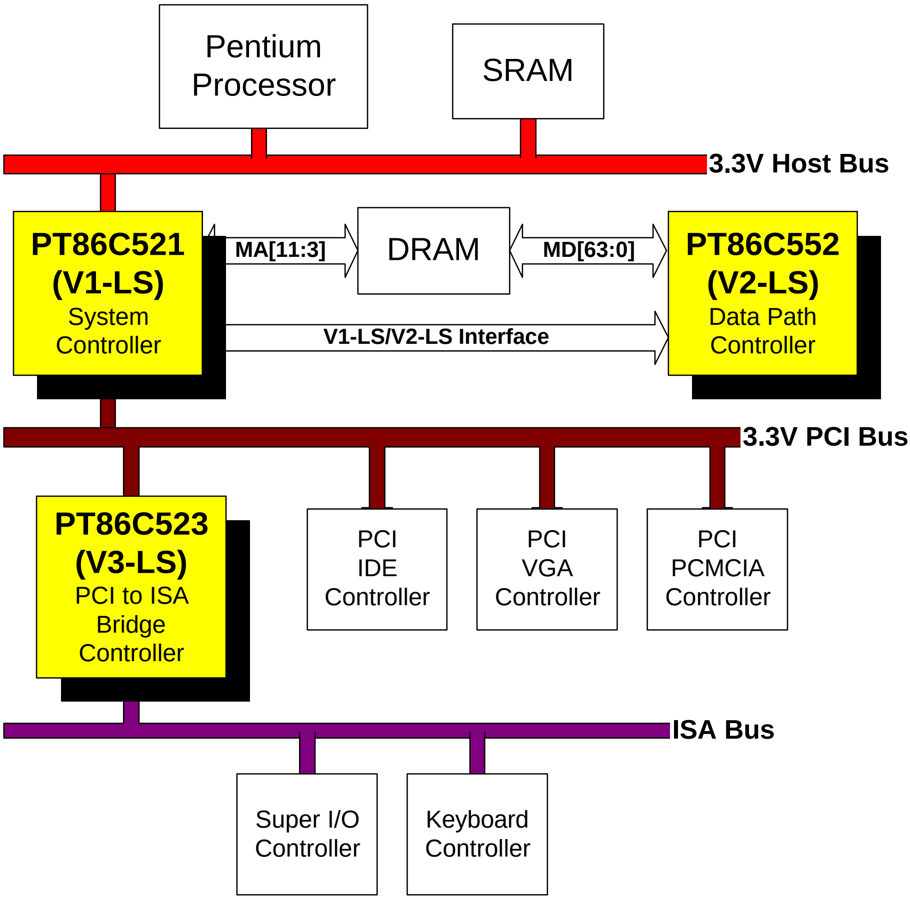


Figure 2-1 Architecture Block Diagram

2.2.1 PT86C521(V1-LS) System Controller

Block Diagram

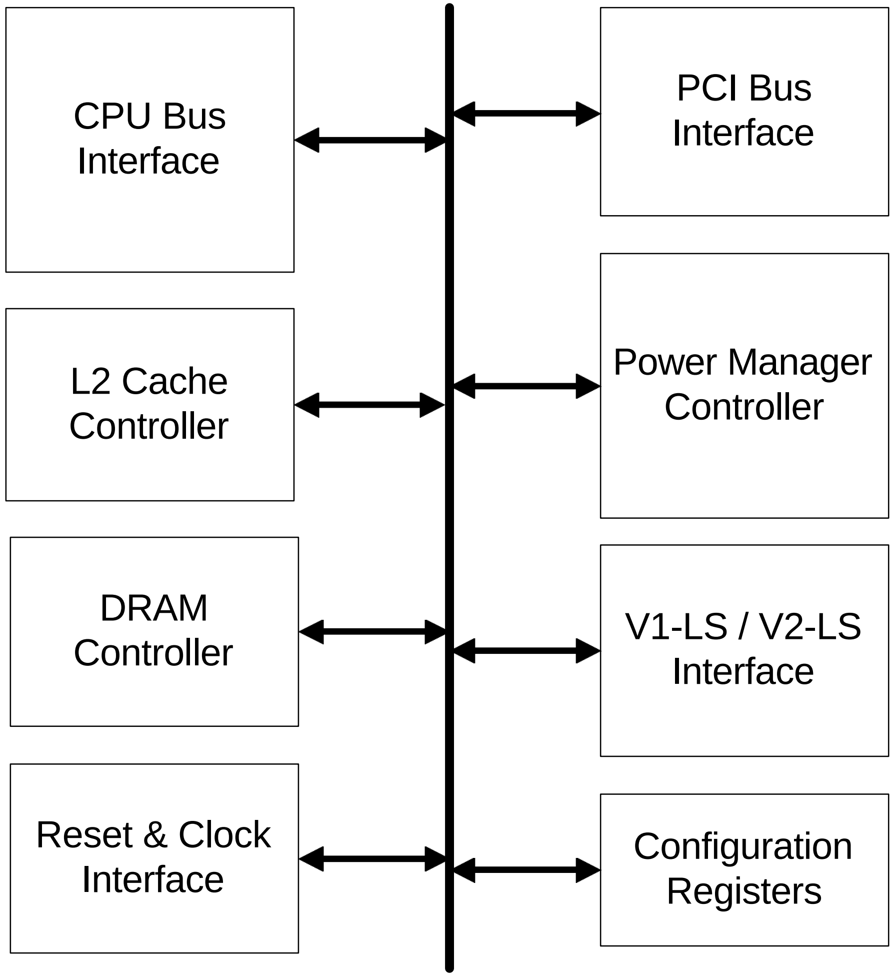


Figure 2-2 PT86C521(V1-LS) Block Diagram

Pin Diagram

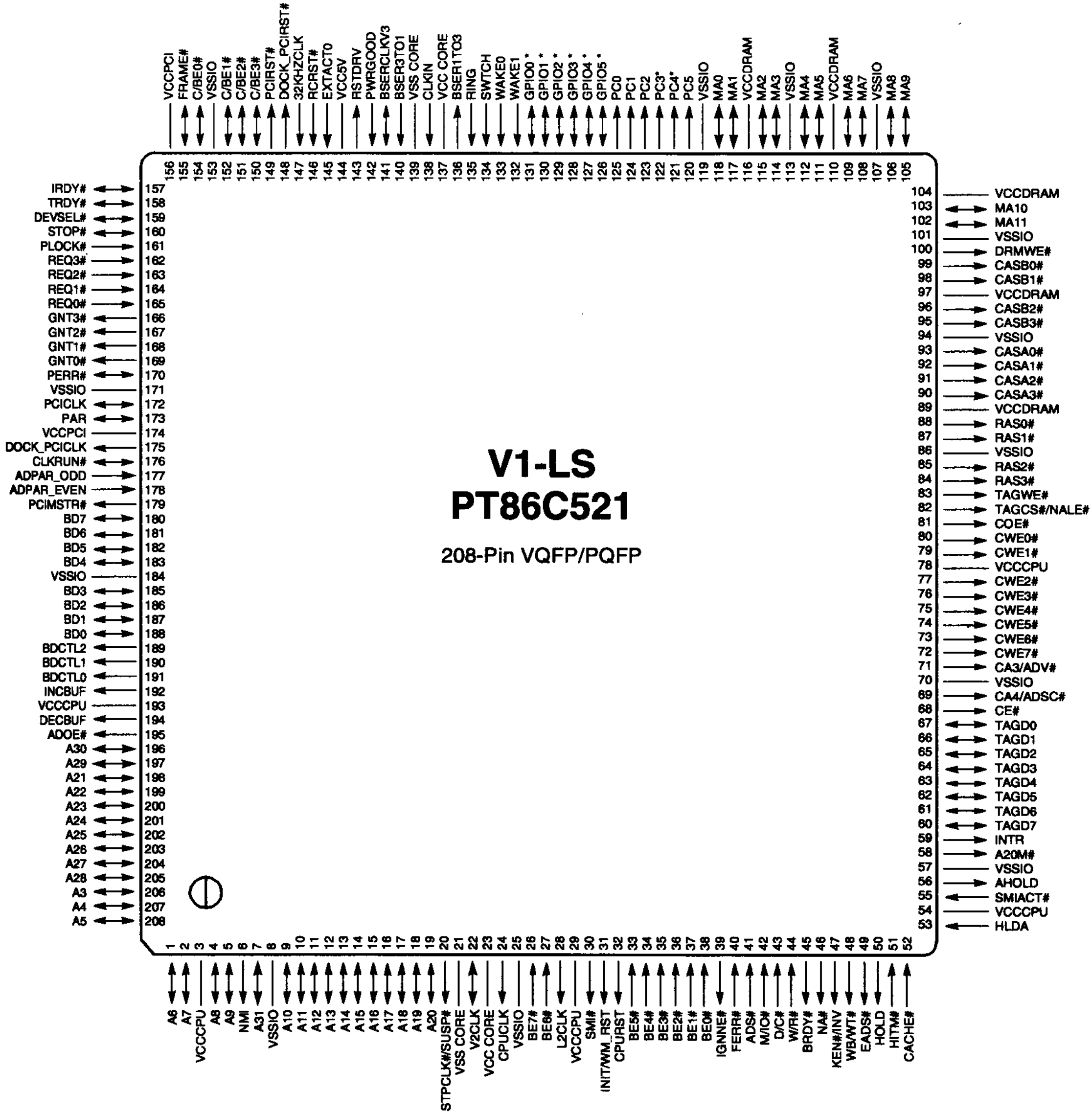


Figure 2-3 PT86C521(V1-LS) Pin Diagram

Pin Descriptions

This section contains a detailed functional description of the pins on V1-LS. For ease of reference, the pins are arranged alphabetically within each of the following functional interface groups:

- CPU Interface (CPU)
- DRAM Interface (DRAM)
- L2 Cache Interface (L2 CACHE)
- PCI Interface (PCI)
- Power Management Interface (PMC)
- V1 -GS / V2-LS Interface (V1-LS / V2-LS)
- V1 -GS / V3-LS Interface (V1 -GS / V3-LS)
- Reset and Clock Interface (RESET / CLOCK)
- Power and Ground (POWER / GROUND)

The '#' symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage. Signal names without the '#' symbol indicate that the signal is active, or asserted at the high voltage level.

The '/' symbol between signal names indicates that the signals are multiplexed or have dual functionality and use the same pin for all functions.

The following conventions have been used to describe the pin type: 'I' = input-only pins; 'O' = output-only pins; and 'I/O' = bi-directional pins. The pin type is defined relative to the Vesuvius platform.

For a list of pins arranged by pin name, refer to the following table.

Table 2-2 V1-LS Pin Descriptions

Pin Name	Pin No.	Type	Description
CPU Interface			
A20M#	58	O	**ADDRESS BIT 20 MASK#:** This output to the CPU indicates that the CPU should mask A20 in order to emulate the 8086 address wrap around.
A[28:3]	205:198, 19:9, 5:1, 208:206	I/O	**CPU ADDRESS LINES [28:3]:** These are address lines that together with the byte enable signals (BE[7:0]) make the address bus and define the physical area of memory or I/O accessed and are driven as outputs during DMA and bus master cycles. **NOTE:** CPU's unused pins [31:29] should be pulled down by 1K-4.7K resistors for proper snooping.

Table 2-2 V1-LS Pin Descriptions (continued)

Pin Name	Pin No.	Type	Description
CPU Interface (continued)			
ADS#	41	I	**ADDRESS STROBE#:** This input indicates the presence of a new valid bus cycle is currently being driven by the CPU. ADS# is driven active in the first clock of a bus cycle and is driven inactive in the second or subsequent clocks of the cycle. ADS# is driven inactive when the bus is idle.
AHOLD	56	O	**ADDRESS HOLD:** This output is used in conjunction with EADS# for write-protecting a cacheable ROM region.
BE[7:0]	26, 27, 33:38	I	**CPU BYTE ENABLE [7:0]:** The byte enable pins are used to determine which bytes must be written to V2-LS memory, or which bytes were requested by the processor for the current cycle. They help define the physical area of the memory or I/O accessed. Byte enable pins are driven in the same clock as ADS#. They are driven with the same timing as the address lines A[28:3].
BRDY#	45	O	**BURST READY#:** This output to the Pentium processor indicates completion of the current cycle. BRDY# indicates that the V2-LS has presented valid data in response to a read, or that it has accepted the data from the Pentium processor in response to a write request.
CACHE#	52	I	**CACHE#:** This input from the Pentium processor indicates a CPU cacheable/burstable operation.
CPUCLK	24	O	**CPU CLOCK OUTPUT:** This will be the clock output from V1-LS to CPU.
CPURST	32	O	**CPU RESET:** This output resets the CPU
D_C#	43		**DATA_CODE#:** This cycle-definition input from the Pentium processor indicates whether the current cycle is a data or a code/special access. The D_C# pin is driven valid in the same clock as ADS# and the cycle address I t remains valid from the clock in which ADS# is asserted until the clock after the earlier of NA# or the last BRDY#.
EADS#	49	O	**EXTERNAL ADDRESS STROBE#:** This output to the Pentium processor indicates that a valid address has been driven onto the CPU address bus for internal cache snoop cycle.
FERR#	40		**FLOATING-POINT ERROR#:** This output pin from the Pentium processor is used for floating-point error reporting.
HITM#	51		**HITM#:** This input indicates that the snoop cycle hit a modified line in the level 1 cache inside the CPU such that V1-LS should suspend the master operation, allow the CPU to evict the modified line, then restart the master cycle.
HLDA	53	I	**HOLD ACKNOWLEDGE:** This output from the Pentium processor indicates a Hold Acknowledge state.
HOLD	50	O	**HOLD REQUEST:** This output to the Pentium processor indicates a Hold Request state.

Table 2-2 V1-LS Pin Descriptions (continued)

Pin Name	Pin No.	Type	Description
CPU Interface (continued)			
IGNNE#	39	O	**IGNORE NUMERIC ERROR#:** This pin indicates that a floating-point error should be ignored.
INIT/WM_RST	31	O	**INIT:** The Pentium processor initialization input forces the Pentium processor to begin execution in a known state. The INITNVM_RST will typically be asserted when software reset commands are written to either Port 64 or 92, or a shutdown cycle is detected. WM_RST: Cyrix M1 processor initialization input forces the processor to begin execution in a known state.
INTR	7	O	**MASKABLE INTERRUPT:** This pin indicates a maskable interrupt request to the Pentium processor.
INV	47	O	See KEN#.
KEN#/INV	47	O	**CACHE ENABLE#:** This output to the Pentium processor indicates that the current cycle is cacheable. INV: This pin indicates a request to invalidate the processor cache line. This output can also be used as INV output during snoop cycles. If this function is not used, CPU's INV pin should either be pulled high or connected to W_R#.
M_IO#	42	I	**MEMORY_INPUT & OUTPUT#:** This cycle-definition signal is one of the main pins that define the bus cycle. It distinguishes a memory access from an I/O access. This signal is driven valid in the same clock as ADS# and the cycle address. It remains valid from the clock in which ADS# is asserted until the clock after earlier of NA# or the last BRDY#.
NA#	46	O	**NEXT ADDRESS#:** NA# indicates to the Pentium processor that V1 GS is ready to accept a new bus cycle.
NMI	6	O	**NON-MASKABLE INTERRUPT:** This pin indicates that an external non-maskable interrupt has been generated.
SMI#	30	O	**SYSTEM MANAGEMENT INTERRUPT#:** This output triggers a system management interrupt and is used to invoke the SMM (system management mode).
SMIACT#	55	I	**SYSTEM MANAGEMENT INTERRUPT ACTIVE#:** This input from the Pentium processor indicates that the CPU is operating In SMM. Assertion of SMIACT# enables remapping of SMRAM to physical DRAM at 000A0000-000BFFFF region.
STPCLK#/ SUSP#	20	O	**STOP CLOCK#:** This output indicates a stop clock request to Intel's Pentium and AMD's K5 processor. SUSP#: This output indicates a suspend request to Cyrix M1 CPU.
SUSP#	20	O	See STPCLK#.

Table 2-2 V1-LS Pin Descriptions (continued)

Pin Name	Pin No.	Type	Description
CPU Interface (continued)			
W/R#	44	I	**WRITE/READ#:** This is a cycle-definition input from the processor indicates whether the current cycle is a write or a read cycle. It is one of the primary bus cycle definition pins. W_R# is driven valid in the same clock as ADS# and the cycle address. It remains valid from the clock in which ADS# is asserted until the clock after earlier of NA# or the last BRDY#.
WB_WT#	48	O	**WRITE-BACK_WRITE-THROUGH#:** This output to the processor allows a data cache line to be defined as write-back or write through on a line-by-line basis.
WM_RST	31	O	See INIT.
DRAM Interface			
CASA[3:0]# CASB[3:0]#	90:93 95:99	O	**COLUMN ADDRESS STROBES l3:0] GROUPS A AND B#:** In 64 bit bank mode, CASA[3:0]# corresponds to BE[3:0]# and CASB[3:0]# corresponds to BE[7:4]#. In 32-bit bank mode CASA[3:0]# outputs drive the CAS# inputs on DRAM bytes 3 to 0 in even banks (banks 0, 2, 4, 6) and odd banks (banks 1, 3, 5, 7).
DRMWE#	100	O	**DRAM WRITE ENABLE#:** This output drives write-enable for all DRAM.
MA[11:0]	102, 103, 105, 106, 108, 109, 111, 112, 114, 115, 117, 118	O	**MEMORY ADDRESSES [11:0]:** These outputs drive MA lines for all DRAM. They are also used as RC-RESET configuration inputs during power up.
RAS[3:0]#	84, 85, 87, 88	O	**ROW ADDRESS STROBES [3:0]#:** These outputs drive the RAS# inputs on DRAM bank pairs 7/6, 5/4, 3/2, and 1/0 respectively.
L2 Cache Interface			
ADSC#	69	O	See CA4.
ADV#	71	O	See CA3.
CA3/ADV#	71	O	**CACHE ADDRESS 3:** Cache Data RAM address bits used for cache burst sequencing with asynchronous SRAM. ADVANCE#: This active low default output is used with synchronous SRAM to advance the internal SRAM burst, counter, controlling burst accesses after the address is loaded.
CA4/ADSC#	69	O	**CACHE ADDRESS 4:** Cache Data RAM address bits used for cache burst sequencing with asynchronous SRAM. ADDRESS STATUS _ONTR;>LLER#: This active low default output is used with synchronous SRAM and interrupts any ongoing SRAM burst, causing a new address to be registered.
CE#	68	O	**CHIP ENABLE#:** Cache data RAM chip enable.
CHITM#	66	I/O	See TAGD1.
COE#	81	O	**CACHE OUTPUT ENABLE#:** Cache Data RAM output enable.

Table 2-2 V1-LS Pin Descriptions (continued)

Pin Name	Pin No.	Type	Description
L2 Cache Interface (continued)			
CWE[7:0]#	72:77, 79, 80	O	**CACHE WRITE ENABLE [7:0]#:** Cache data RAM byte write enables.
L2CLK	28	O	**L2 CLOCK:** Clock output to synchronous cache data RAM.
MATCH#	67	I/O	See TAGD0.
NALE#	59	O	**NEXT ADDRESS LATCH ENABLE#:** When not using synchronous SRAM, this output controls an external latch for the cache addresses necessary for pipelining.
SONY_KEN#	65	I/O	See TAGD2.
TAGCS#	82	O	**TAG RAM CHIP SELECT#:** TAG Data RAM chip select.
TAGD0/ MATCH#	67	I/O	**TAG RAM Data Bit 0#:** Used to compare addresses from the Pentium processor to determine L2 Cache cycles. MATCH#: Match input from external TAG SRAM.
TAGD1/ CHITM#	66	I/O	**TAG RAM Data Bit [1]:** Used to compare addresses from the Pentium processor to determine L2 Cache cycles. CHITM#: Input from SONY's Sonic-2WP.
TAGD2/ SONY_KEN#	65	I/O	**TAG RAM DATA BIT 2:** Used to compare addresses from the Pentium processor to determine L2 Cache cycles. SONY_KEN#: Output to SONY's Sonyc-2WP.
TAGD[7:3]#	60:64	I/O	**TAG RAM DATA BITS [7:3l:** Used to compare addresses from the Pentium processor to determine L2 Cache cycles.
TAGWE#	83	O	**TAG RAM WRITE ENABLE#:** TAG Data RAM write enable.
PCI Interface			
BE[3:0]#	35:38	I/O	See C[3:0]#.
C/BE[3:0]#	150, 151, 152, 154	I/O	**BUS COMMAND/BYTE ENABLES [3:0]#:** Both are multiplexed on the same PCI pins. These pins define the Bus Command during the address phase and are used as Byte Enables during the data phase.
DEVSEL#	159	I/O	**DEVICE SELECT#:** As an output it indicates whether V1-LS system memory is the target of the current address. As an input, V1-LS sees whether or not a PCI target exists.
FRAME#	155	I/O	**FRAME#:** FRAME# is driven by the current initiator and indicates the start and duration of the transaction. FRAME# is deasserted to indicate that the initiator is ready to complete the final data phase. A transaction may consist of one or more data transfers between the current initiator and the currently-addressed target.
GNT[3:0]#	166, 169	O	**PCI GRANT [3:0]#:** When the bus arbiter has granted access to the aster requesting the ownership of the PCI bus, the master is notified using this point to point signal. Each PCI bus master has its own GNT#.

Table 2-2 V1-LS Pin Descriptions (continued)

Pin Name	Pin No.	Type	Description
PCI Interface (continued)			
IRDY#	157	I/O	**INITIATOR READY#:** This indicates the bus master's state of readiness to complete the current data phase. During a write, IRDY# shows that valid data is present. During a read, it indicates the bus master's readiness to accept data. IRDY# is used in conjunction with TRDY#.
PAR	173	I/O	**PARITY:** All PCI agents require parity generation.
PCICLK	172	I/O	**PCI CLOCK:** This pin provides timing for all transactions on the PCI bus.
PCIRST#	178	O	**PCI RESET:** This signal when asserted resets all PCI devices.
PERR#	170	I	**PARITYERROR#:** This input indicates a data parity error. It may be pulsed active by any agent that detects an error condition.
PLOCK#	161	I/O	**PLOCK#:** This signal allows the master to lock the PCI bus and the arbiter does not grant the PCI bus to a new master until this signal has been deasserted.
REQ[3:0]#	162:165	I	**PCI REQUEST[3:0]#:** This signal indicates to the arbiter that this agent requests use of the bus. This is a point-to-point signal. Every PCI bus master has its own REQ#.
STOP#	160	I/O	**STOP#:** This signal facilitates either master abort or target abort cycles.
TRDY#	158	I/O	**TARGET READY#:** This indicates the ability of the target device to complete the current data phase of the bus transaction. During a read phase, TRDY# indicates that the valid data is present. During a write phase, it indicates that the device is prepared to accept data.
Power Management Controller Interface			
DOCKED	128	I/O	See GPIO3.
DOCK_START	129	I/O	See GPIO2
EXTACT[1:0]	148, 149	I	**EXTERNAL ACTIVITY[1:0]:** These pins indicate that there is current external activity.
GPIO0/LED0	131	I/O	**GENERALPURPOSE I/O:** This pin can also be selected as a general purpose pin. Its function can be enabled by index register 352H, bit 0. LED0: LED indicator output 1.
GPIO1/LED1/	130	I/O	**GENERAL PURPOSE I/O 1#:** This pin can also be selected as a general purpose pin. Its function can be enabled by index register 352H, bits [2:1]. LED 1#: LED indicator output 1.
SUSPA#	130		**SUSPEND ACKNOWLEDGE#:** This output from the Cyrix M1 CPU indicates a suspend acknowledge state.
GPIO2/ DOCK_START	129	I/O	**GENERAL PURPOSE I/O 2:** This pin can also be selected as a general purpose pin. Its function can be enabled by index register 352H, bit 3. DOCKING START: This pin indicates that docking has started.

Table 2-2 V1-LS Pin Descriptions (continued)

Pin Name	Pin No.	Type	Description
Power Management Controller Interface (continued)			
GPIO3/ DOCKED	128	I/O	**GENERAL PURPOSE I/O 3:** This pin can also be selected as a general purpose pin. Its function can be enabled by index register 352H, bit 4. DOCKED: This pin indicates that docking is complete.
GPIO4/ UNDOCKING	127	I/O	**GENERAL PURPOSE I/O 4:** This pin can also be selected as a general purpose pin. Its function can be enabled by index register 352H, bit 5. UNDOCKING: This pin indicates that undocking has started.
GPIO5/ THERM	126	I/O	**GENERAL PURPOSE I/O 5#:** This pin can also be selected as a general purpose pin. Its function can be enabled by index register 352H, bits [7:6]. THERMAL SENSOR INPUT#: This input allows an external thermal sensor to feed thermal information back to the thermal throttler to regulate the control of heat generated by the CPU.
LED0	131, 122	I/O	See GPIO0 and PC3.
LED1	130, 121	I/O	See GPIO1 and PC4.
PC[2:0]	123:125	0	**POWER CONTROL [2:0]:** This output provides individual power control for any system component.
PC3/LED0	122	O	**POWER CONTROL 3:** This output provides individual power control for any system component. LED 0: LED indicator output 0.
PC4/LED1	121	O	**POWER CONTROL 4:** This output provides individual power control for any system component. LED 1: LED indicator output 1.
PC5	120		**POWER CONTROL 5:** This output provides individual power control for any system component.
RING	135	I	**RING:** This input provides for a wake-up' call from a modem.
SUSPA#	130	I/O	See GPIO1.
THERM	126	I/O	See GPIO5.
UNDOCKING	127	I/O	See GPIO4.
WAKE[1:0]	132, 133	I	**WAKE [1:0]:** These pins request V1-LS to: (a) power-up the system and initiate a “resume" operation if the system was previously in Suspend mode, or (b) cold boot if the system was previously in the Standby mode or was powered down.
V1-LS / V2-LS Interface			
ADOE#	195	O	**AD BUS OUTPUT ENABLE#:** When this signal is active V2-LS drives the PCI AD bus AD[31:0]
ADPAR_ODD	196	I/O	**ODD AD BUS PARITY:** Input from V2-LS to indicate PCI AD Bus parity.
ADPAR_EVEN	197	I/O	**EVEN AD BUS PARITY:** Input from V2-LS to indicate PCI AD Bus parity.
BD[7:0]	180:183, 185:188	I/O	**BURST DATA BUS [7:0]:** This 8-bit bus carries different information during various phases between V1-LS and V2-LS.

Table 2-2 V1-LS Pin Descriptions (continued)

Pin Name	Pin No.	Type	Description
V1-LS / V2-LS Interface (continued)			
BDCTL[2:0]	189:191	0	**BDCTL[2:0]:** Data path control signals to V2-LS.
DECBUF	194	O	**DECREMENT WRITE BUFFER COUNTER:** This output is used to decrease the pointer on the eight-level write buffer.
INCBUF	192	O	**INCREMENT WRITE BUFFER COUNTER:** This output is used to increase the pointer on the eight-level write buffer.
PCIMSTR#	179	O	**PCI MASTER#:** Indicates to V2-LS that V1-LS is responding to a PCI master cycle.
V2CLK	22	O	**V2 CLOCK:** Clock for the interface between V1-LS and V2-LS.
V1-LS / V3-LS Interface			
BSER1TO3	141	O	**SERIAL BUS:** Serial bus interface from V1-LS to V3-LS.
BSER3TO1	140	I	**SERIAL BUS:** Serial bus interface from V3-LS to V1-LS.
Reset and Clock Interface			
32KHZCK	147	I	**CLOCK:** Clock source used for DRAM controller and power management functions.
CLKIN	138	I	**CLOCK:** Input clock source to CPU clock. CMOS level 50/5- duty cycle is recommended.
BSERCLKV3	141	O	**CLOCK:** Clock for the serial interface between V1-LS and V3-LS.
PWRGOOD	142	I	**POWER GOOD INPUT:** This input causes a complete system reset. It is driven by the PWRGOOD signal from the power supply or a reset switch. On power up, PWRGOOD going from low to high indicates that external VCC is stable and will wake up V1-LS from Standby to On. If PWRGOOD goes low, it will drive the chip back to Standby.
RCRST#	146	I	**RC RESET#:** This input is used to reset V1-LS' power management controller upon initial system power-up. It should have a pull-up resistor tied to the same power source as V1-LS.
RSTDRV	143	O	**AT BUS RESET OUTPUT:** This output provides a system reset
SPNDNRST	145	O	**SUSPEND NOT RESET:** This output provides a reset equivalent to RSTDRV except when in Suspend Mode. During Resume SPNDNRST will not pulse so that any device not powered down during Suspend Mode should use this reset. **NOTE:** Do not connect thin pin for V1-LS; this pin is only applicable to V1

Table 2-2 V1-LS Pin Descriptions (continued)

Pin Name	Pin No.	Type	Description
Power and Ground			
VCC5-V	144	PWR	VCC5-V
VCCCORE	23, 137	PWR	VCCCORE
VCCCPU	3, 29, 54, 78, 193	PWR	VCCCPU
VCCDRAM	89, 97, 194, 110, 116	PWR	VCCDRAM
VCCPCI	156, 174	PWR	VCCPCI
VSSCORE	21, 139	PWR	VSSC
VSSIO	8, 25, 57, 70, 86, 94, 101, 107, 113, 119, 153, 171, 184,	GND	VSSIO

2.2.2 PT86C522(V2-LS) Data Path Controller

Block Diagram

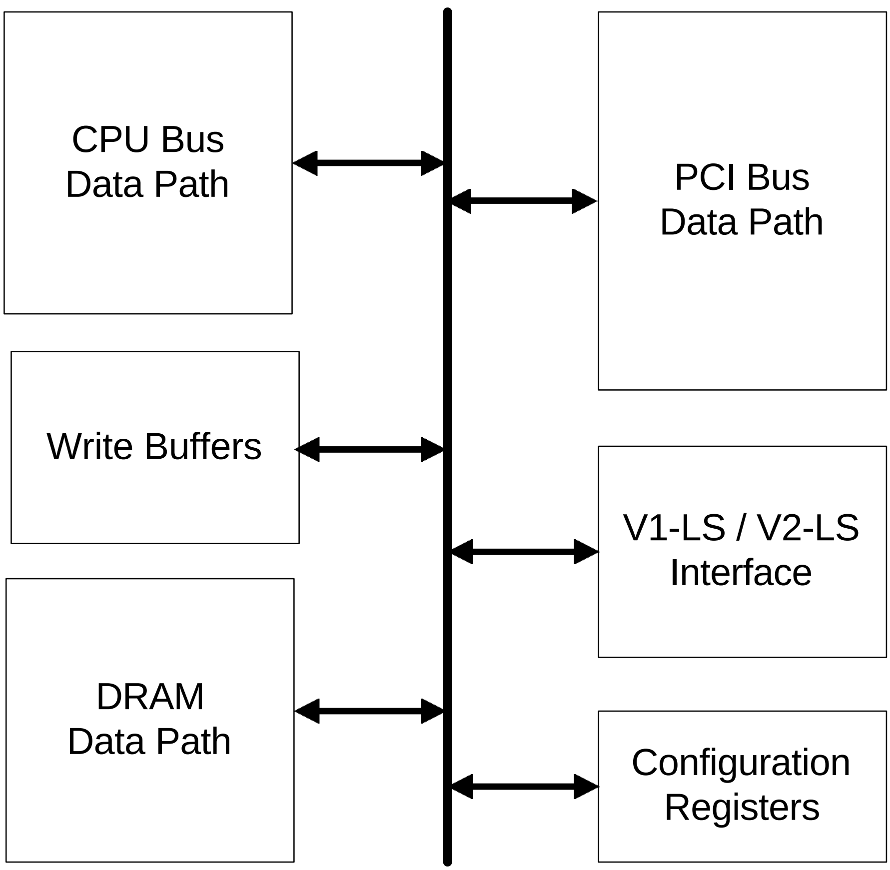


Figure 2-4 PT86C522(V2-LS) Block Diagram

Pin Diagram

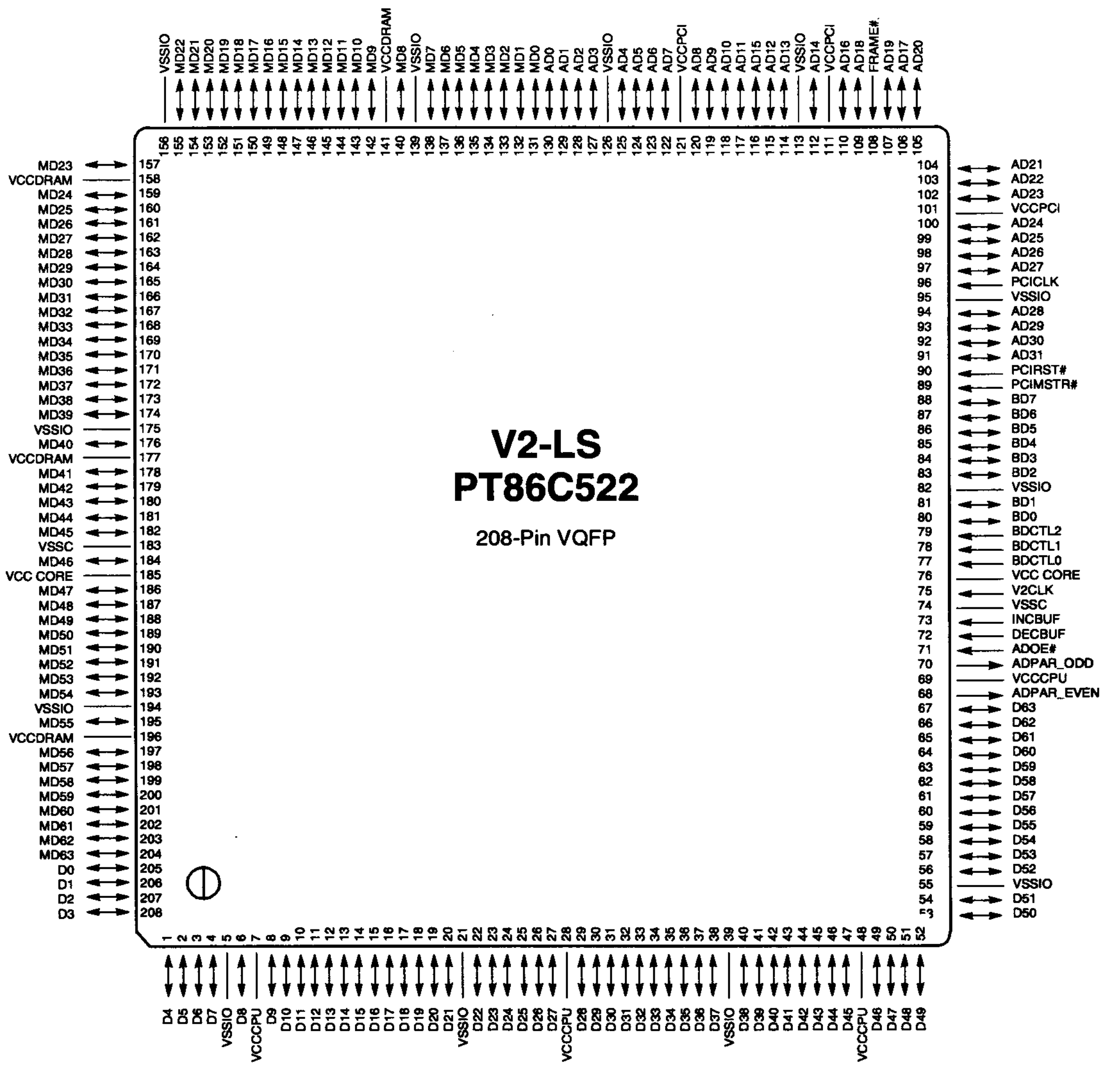


Figure 2-5 PT86C522(V2-LS) Pin Diagram

Pin Descriptions

This section contains detailed functional description of the pins on V2-LS. For ease of reference, the pins have been arranged alphabetically within each of the following functional interface groups:

- CPU Interface (CPU)
- DRAM Interface (DRAM)
- PCI Interface (PCI)
- V1-LS/V2-LS Interface (V1 -GS / V2-LS)
- Power and Ground (POWER / GROUND)

The '#' symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage. Signal names without the # symbol indicate that the signal is active, or asserted at the high voltage level.

The '/' symbol between signal names indicates that the signals are multiplexed and use the same pin for all functions.

The following conventions have been used to describe the pin type: 'I' = input-only pins; 'O' = output-only pins; and 'I/O' = bi-directional pins. The pin type is defined relative to the Vesuvius platform.

For a list of pins arranged by pin name, refer to the following table.

Table 2-3 V2-LS Pin Descriptions

Pin Name	Pin No.	Type	Description
CPU Interface			
D[63:0]	67:40, 38:22, 20:8, 6, 4:1, 208:205	I/O	**CPU DATA BUS D[63:0]:** These are the upper and lower bits of the 64-bit Pentium processor data bus.
DRAM Interface			
MD[63:0]	204:195, 193:186, 184, 182:178, 176, 174:159, 157, 155:142, 140, 138:131	I/O	**DRAM DATA BUS:** These pins are dedicated DRAM array data pins. These pins are inputs during DRAM read cycles and outputs during DRAM write cycles.
PCI Interface			
AD[31:0]	91:94, 97:100, 1012:105, 107, 109:115, 117:120, 122:125, 127:130	I/O	**ADDRESS/DATA MULTIPLEXED [31:0]:** These signals are multiplexed on the same pins. Each transaction is initiated by a 32-bit physical address phase which is followed by one or more data phases. These bus transactions support both read and write bursts. AD[31:0] are also used as IDSELs in the Configuration Cycle.
FRAME#	108	I	**FRAME#:** FRAME# is driven by the current initiator and indicates the start and duration of the transaction. FRAME# is deasserted to indicate that the initiator is ready to complete the final data phase. A transaction may consist of one or more data transfers between the current initiator and the currently-addresses target.

Table 2-3 V2-LS Pin Descriptions

Pin Name	Pin No.	Type	Description
PCI Interface (continued)			
PCICLK	96	I	**PCI CLOCK INPUT:** This is a clock generated by V1-LS and is derived from LCLK and delayed by 1/2+ clock cycle or is the inversion of LCLK.
PCIRST#	90	I	**PCI RESET:** This signal is the PCI reset signal
V1-LS/V2-LS Interface			
ADOE#	71	I	**AD BUS OUTPUT ENABLE#:** When this signal is active, V2-LS drives the PCI AD bus AD[31:0].
ADPAR_EVEN	68	I/O	**AD BUS PARITY:** This signal indicates the PCI AD Bus parity when V2-LS samples PCI AD Bus.
ADPAR_ODD	70	I/O	**AD BUS PARITY:** Output to V1-LS to indicate PCI AD Bus parity.
BD[7:0]	88:83, 81, 80	I/O	**BURST DATA BUS [7:0]:** This 8-bit bus carries different information during various phases.
BDCTL[2:0]	79:77	I	**BDCTL[2:0]:** Datapath control signals from V1-LS
DECBUF	72	-- I	**DECREMENT WRITE BUFFER COUNTER:** This input is used to decrease the pointer on the 8 level write buffer.
INCBUF	73	I	**INCREMENT WRITE BUFFER COUNTER:** This input is used to increase the pointer on the 8 level write buffer.
PCIMSTR#	89	I	**PCI MASTER#:** This output from V1-LS indicates that Vesuvius is responding to a PCI master cycle.
Power and Ground			
VCCC	76, 185	PWR	VCCC
VCCCPU	7, 28, 48, 69, 158, 177, 196	PWR	VCCCPU
VCCDRAM	141	PWR	VCCDRAM
VCCPCI	101, 121	PWR	VCCPCI
VSSIO	5, 21, 39, 55, 82, 95, 106, 116, 126, 139, 156, 175, 194,	GND	VSSIO
VSSC	74, 183	GND	VSSC

2.2.3 PT86C521(V3-LS) PCI to ISA Controller

Block Diagram

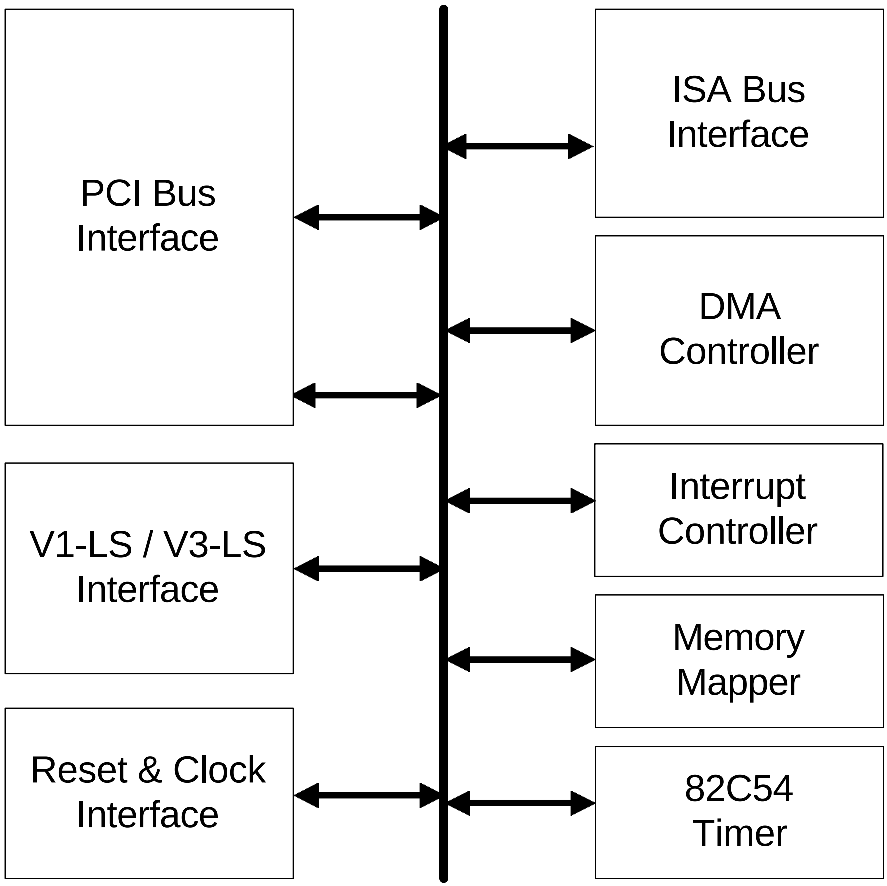


Figure 2-6 PT86C521(V3-LS) Block Diagram

Pin Diagram

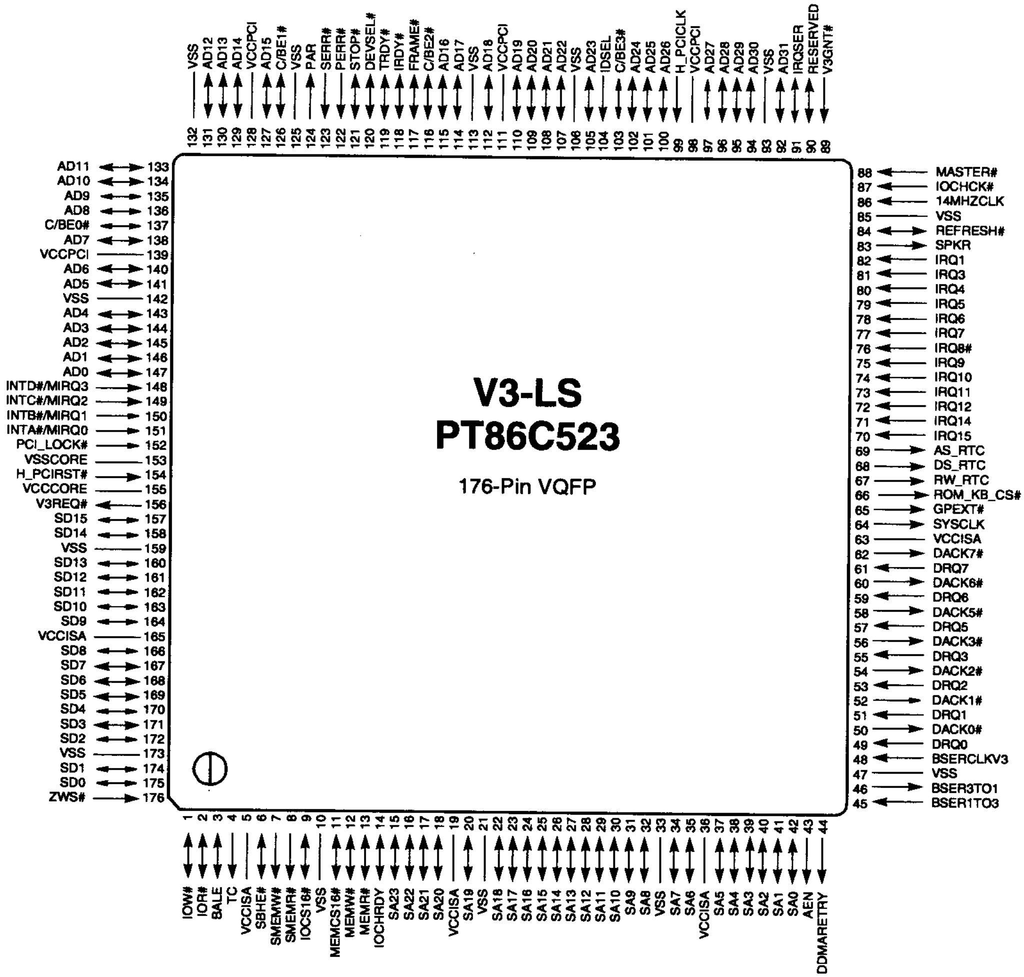


Figure 2-7 PT86C521(V3-LS) Pin Diagram

Pin Descriptions

This chapter contains a detailed functional description of the pins on V3-LS. For ease of reference, the pins have been arranged alphabetically within each of the following functional interface groups:

- ISA Interface (ISA)
- PCI Interface (PCI)
- Power and Ground (POWER/GROUND)

The '#' symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage. Signal names without the # symbol indicate that the signal is active, or asserted at the high voltage level.

The '/' symbol between signal names indicates that the signals are multiplexed and use the same pin for all functions.

The following conventions indicate the pin type: 'I' = input-only pins; 'O' = output-only pins; and 'I/O' = bidirectional pins. The pin type is defined relative to the Vesuvius platform.

For a list of pins arranged by pin name, refer to the following table.

Table 2-4 V3-LS Pin Descriptions

Pin Name	Pin No.	Type	Description
ISA Interface			
AEN	43	O	**ADDRESS ENABLE:** If AEN is driven high, it indicates that the DMA controller has taken control of the CPU address bus and the AT bus command lines.
AS_RTC	69	O	**RTC ADDRESS STROBE:** This output should be connected to the AS_RTC input of an 146818-type or equivalent RTC.
ATFLOAT#	87	I	**ATFLOAT#:** This pin is multiplexed with IOCHCK#. If the ATFLOAT# pin function is enabled through register ATCR-2 bit 2. Then driving ATFLOAT# low will float the ISA bus. This function is to facilitate ISA hot docking design. Docking operation details: TBD.
BALE	3	I/O	**BUFFERED ADDRESS LATCH ENABLE:** This output is driven to the AT bus where it indicates the presence of a valid address on the bus.
BSERCLKV3	48	I	Burst bus clock for serial system and power management bus.
BSER1TO3	45	I	Serialized system & power management information from V1-LS to V3-LS.
BSER3TO1	46	O	Serialized system & power management information from V3-LS to V1 -GS
CLK14MHZ	86	I	14.318 MHz clock for the 8254 timer.
DACK[7:5, 3:0]#	62, 60, 58, 56, 54, 52, 50	O	**DMA ACKNOWLEDGE [7:5, 3:0]#:** DACKn# asserted indicates the corresponding DMA channel request "n" has been granted.
DRQ[7:5, 3:0]	61, 59, 57, 55, 53, 51, 48	I	**DMA REQUEST [7:5, 3:0]#:** DRQn asserted indicates a DMA device is requesting DMA service using Channel "n".
DS_RTC	68	O	**RTC DATA STROBE:** This output should be connected to the DS_RTC input of an 14681 8-type or equivalent RTC.

Table 2-4 V3-LS Pin Descriptions (continued)

Pin Name	Pin No.	Type	Description
ISA Interface (continued)			
GPEXT#	65	O	**GENERAL PURPOSE OUTPUT EXTENSION:** The GPEXT# is pulsed (low) when register GPEXT_LB is being written. The value being written to GPEXT_LB and the value previously latched in GPEXT_HB will be driven onto SD[7:0] and SD[15:8] respectively to extend by up to 16 general purpose outputs. An external 8-bit or 16-bit flip-flop should be used to latch the SD-bus on the rising (trailing) edge of GPEXT#.
IOCHCK#	87	I	**UO CHANNEL CHECK:** This input indicates a parity error from some device on the AT bus. This pin is multiplexed with ATFLOAT#.
IOCHRDY	14	I/O	**UO CHANNEL READY:** When this input is driven low, it indicates that the device on the AT bus currently being accessed requires additional time to complete the cycle.
IOCS16#	9	I/O	**I/O CHIP SELECT 16#:** This input from the AT bus indicates that the current access is to a 1 6-bit I/O device.
IOR#	2	I/O	**I/O READ#:** This output to the AT bus indicates an I/O Read cycle.
IOW#	1	I/O	**I/O WRITE#:** This output to the AT bus indicates an I/O Write cycle.
IRQ[15,14,12:3,1]	70, 71, 72:82	I	**INTERRUPT REQUEST:** ISA bus interrupt requests.
MASTER#	88	I	**MASTER#:** This input from the AT bus indicates that a slot master has taken control of the AT bus.
MEMCS16#	11	I/O	**MEMORY CHIP SELECT 16-BIT#:** This input from the AT bus indicates that the current access is to a 16-bit memory device.
MEMR#	13	I/O	**MEMORY READ#:** This output to the AT bus indicates a Memory Read cycle to any valid AT bus address.
MEMW#	12	I/O	**MEMORY WRITE#:** This output to the AT bus indicates a Memory Write cycle to any valid AT bus address.
REFRESH#	84	I/O	**REFRESH#:** This output drives the AT bus to indicate a Memory Refresh cycle.
ROM_KB_CS#	66	O	Combined system BIOS, keyboard, and chip select output.
RW_RTC	67	O	**RTC READ/WRITE:** This output should be connected to the RW_RTC input of an 14681 8-type or equivalent RTC.
SA[23:0]	15:18, 20, 22, 23:32, 34, 35, 37:42	I/O	**SLOT ADDRESS[23:0]:** These signals are decoded from AD[31:0] and BE[3:0]# of PCI bus. These signals will become inputs during ISA master cycles and will be outputs during all other cycles.
SBHE#	6	I/O	**SLOT BYTE HIGH ENABLE#:** This output to the AT bus indicates a data transfer on the high byte of the SD bus.

Table 2-4 V3-LS Pin Descriptions (continued)

Pin Name	Pin No.	Type	Description
ISA Interface (continued)			
SD[15:0]	157, 158, 160:164, 166:172, 174, 175	I/O	**SLOT DATA[15:0]:** These I/Os are the data read and write path for the AT bus.
SMEMR#	8	O	**SLOT MEMORY READ#:** This output to the AT bus indicates that a Memory Read cycle is within the lower 1 Mbyte address range.
SMEMW#	7	O	**SLOT MEMORY WRITE#:** This output to the AT bus indicates that a Memory Write cycle is within the lower 1 Mbyte address range.
SPKR	83	O	**SPEAKER:** Speaker data output.
SYSCLK	64	O	SYSTEM CLOCK: AT bus clock. It is derived from BSERCLKV3 and the divisor is selectable by register ATCR-1 bit [2:0].
TC	4	O	**TERMINAL COUNT:** Signal on the ISA bus indicating that a terminal count has reached for a given channel.
ZWS#	176	I	**ZERO WAIT STATE#:** This input from the AT bus indicates that the device currently being accessed can complete the cycle with zero wait states
PCI Interface			
AD[31:0]	92, 94:97, 100:102, 105, 107:110, 112, 114, 115, 127, 129:131, 133:136, 138, 140, 141, 143:147	I/O	**ADDRESS/DATA MULTIPLEXED [31:0]:** These signals are multiplexed on the same pins. Each transaction is initiated by a 32-bit physical address phase which is followed by one or more data phases. These bus transactions support both read and write bursts.
C/BE[3:0]#	103, 116, 126, 137	I/O	**COMMAND/BYTE ENABLES [3:0]#:** Both are multiplexed on the same pins. The pins define the Bus Command during the address phase. During the data phase, the pins are used as Byte Enables.
DEVSEL#	120	I/O	**DEVICE SELECT#:** As an output it indicates whether Vesuvius is the target of the current address. As an input, Vesuvius sees whether or not a PCI target exists.

Table 2-4 V3-LS Pin Descriptions (continued)

Pin Name	Pin No.	Type	Description
PCI Interface (continued)			
FRAME#	117	I/O	**CYCLE FRAME#:** Cycle Frame is driven by the current initiator and indicates the start and duration of the transaction. FRAME# is deasserted to indicate that the initiator is ready to complete the final data phase. A transaction may consist of one or more data transfers between the current initiator and the currently-addresses target.
H_PCICLK	99	I	**PCI CLOCK:** 33/25 MHz clock for the PCI bus.
H_PCIRST#	154	I	**PCI RESET:** V3-LS reset input.
IDSEL	104	I	**ID SELECT:** ID Select for PCI interrupts.
IRDY#	118	I/O	**INITIATOR READY#:** This indicates the bus master's state of readiness to complete the current data phase. During a write, IRDY# shows that valid data is present. During a read, it indicates the bus master's readiness to accept data. IRDY# is used in conjunction with TRDY#.
PCI_LOCK#	152	I	**PCI LOCK#:** Used for locking ISA resources.
PAR	124	I/O	**PARITY:** All PCI agents require parity generation.
PCI_INT[D:A]#	148:151	I	**PCI INTERRUPTS [D:A]#:** These inputs from PCI devices are shareable, level sensitive (active low) interrupt request. They can be mapped to ISA IRQx through registers PINTM-1 and PINTM-2.
PERR#	122	I	**PARITY ERROR#:** This input indicates a data parity error. It may be pulsed active by any agent that detects an parity error condition.
SERR#	123	I	**SYSTEM ERROR#:** This input may be pulsed active by any agent that selects any system error condition.
STOP#	121	I/O	**STOP#:** This allows the master to stop the bus transaction to the current target device.
TRDY#	119	I/O	**TARGET READY#:** This indicates the ability of the target device to complete the current data phase of the bus transaction. During a read phase, TRDY# indicates that the valid data is present. During a write phase, it indicates that the device is prepared to accept data
Power and Ground			
VSS	10, 21, 33, 47, 85, 93, 106, 113, 125, 132, 152, 159, 173	GND	VSS
VSSCORE	153	GND	VSSCORE
VCCCORE	155	PWR	VCCORE
VCCISA	5, 19, 36, 63, 165	PWR	VCCISA
VCCPCI	98, 111, 128, 139	PWR	VCCPCI

2.3 NM2090 Video Controller

The NM2090 is a high performance Flat Panel Video Accelerator that integrates in one single chip, High Speed DRAM, 24-bit true-color RAMDAC, Graphics/Video Accelerator, Dual clock synthesizer and a high speed glueless 32-bit PCI and VL bus interface.

By integrating the display DRAM and 128-bit graphics/video accelerator, the NM2090 achieves the highest performance of any notebook graphics controller. Delivering over 400MB/s of bandwidth, the NM2090 has sufficient bandwidth to perform full-screen, 30fps video acceleration of MPEG, Indeo, Cinepak, and other video playback CODECs. The bandwidth headroom also allows the NM2090 to deliver the highest quality video playback of any notebook graphics solution, without compromising simultaneous graphics performance.

The unique integration of the NM2090also allows the NM2090to consume 70% less power than equivalent video solutions, with fewer chips and less board space.

The NM2090 Accelerated Super VGA Flat Panel Controller is the solution for the ultimate design goals of mobile computers providing the highest performance, lowest power consumption and the smallest PCB footprint. This is accomplished by integrating the display controller logic and display memory into one chip, and allows system designers to meet all their design goals without having to make any compromises between power and performance. A wide variety of LCD panels are supported, including SVGA (800x600) at 64K colors in a single chip. The CRT/TFT panels can be driven up to a resolution of 1024x768 NI to provide a wide range of feature selection without redesign.

NM2090 delivers very high performance using integration and architectural advances. The integrated DRAM is configured with a 128-bit wide data path, providing very high bandwidth for the CRT, LCD, BitBLT, Video engine and CPU to use. The on-chip DRAM allows flexible DRAM controls adding into overall performance. The integration of the display memory offers lowest power consumption among all implementations of comparable performance and memory capacity. NM2090 keeps system designers free of all the issues regarding memory design for performance, power, EMI radiation and board space. The display memory integration provides the lowest chip count solution for space saving and packaging flexibility.

NM2090 supports 32-bit VL and PCI high performance. Buses to interface with the system. The PCI interface is designed to be fully compliant with the revision 2.0 PCI specification. Both PCI and VL modes support 0 wait state write burst cycles to ensure fast writes into the graphics subsystem. The bus interface can be independently operated at 3.3V;.o8YLjfcirtXwer savings.

NM2090 incorporates GUI acceleration features to further increase the graphics performance. It supports 64-bit BLT for screen-to-screen and host-to-screen operations. Memory mapped I/O and linear addressing allows faster updates into. the graphics subsystem. It also supports color expansion, Clipping, X-Y Coordinates Addressing, Text Acceleration, hardware cursor and icon.

To accelerate video playback under Graphical User interface (GUIs) such as Windows95®, The NM2090 has Color Space Conversion, Horizontal and Vertical Scaling, and Filtering built in the hardware to accelerate video overlay on the graphics screen. Both alpha key and color key are supported for overlay control. NM2090 is packaged in a low profile 176 pin TQFD package.

NM2090 supports complete power management features to reduce the graphics subsystem power and increase the battery life of the portables. The core of NM2090 is always running at 3.3V to reduce the power consumed. All of the interface including bus, panel and VAFC can be operated independently at 3.3V or SV. This allows designers a glueless mixed voltage systems. Different power saving modes are supported under hardware or software controls. NM2090 internally switches off clocks that are not in use to reduce the power transparently. Also, sections of the chip such as DAC can be shut down to save power.

A wide range of VGA and SVGA panels are supported. The panel interface can be selected for 3.3V or SV. Frame rate control and dithering techniques are used for gray scales display. Vertical and horizontal expansion and centering of video displays are supported on all the LCD panel resolutions. Text mode contrast is enhanced using foreground/background technique. In order to reduce the EMI radiation programmable drives are provided on the panel interface signals to match the drive requirements from the panel manufacturers. Simultaneous display on CRT and LCD panel are supported for all types of panels.

lntegrated RAMDAC offers low power and low board space. It contains 256X24 word palette for color selection. The triple 8-bit DACs run up to 80 MHz at 3.3V. NM2090 supports two integrated programmable frequency synthesizers to generate memory and video clock. The clock synthesizers can be turned off for power savings. VAFC compatible video interface is supported in 16-bit for VL bus and

2.3.1 Features

128 Bit Graphics Acceleration

- High speed BitBLT Engine.
- Color Expansion
- Accelerated Text Hardware.
- Clipping.
- X-Y Coordinates Addressing.
- Memory Mapped I/O.
- Up to 2X performance boost over NM2070

Video Acceleration

- Integrated frame buffer for Video and Graphics
- Color Space Conversion (YUV to RGB)
- Arbitrary video scaling up to 8X ratio.
- Bilinear interpolation and Filtering
- Video Overlay capability from on/off screen memory.
- Chroma Key Support
- Independent Brightness Control for Video Window.

- Mixed color depth Video and Graphics.
- Supports different color depths between video and graphics.
- Supports RGB graphics and video in YUV format in one Integrated frame buffer.

Memory Support

- High Speed integrated DRAM.
- 128 bit Memory Interface.
- Over 400MB/s memory bandwidth.

Bus Support

- PCI Local Bus (Zero wait states).
- VESA VL-Bus (Zero wait states).
- 3.3Volts or 5Volts operation.

Hardware Cursor and Icon.

- 64 X 64 Hardware Cursor
- 64 X 64 or 128 X 128 Hardware Icon

Green PC Support

- VESA Display power Management (DPMS).
- DAC Power Down modes.
- Suspend / Standby / Clock management.
- VGA disable support.
- PCI Mobile Computing "clockrun" support.

Resolution and Color Support

- VGA: TFT, DSTN, CRT @ 85Hz (640 X 480 256, 64k, 16M).
- SVGA: TFT, DSTN, CRT @ 85Hz (800X600 256,64k).
- Supports 800x600x64K colors DSTN panels in a single chip!
- XGA: TFT, CRT @ 75Hz (1024 X 768 256 Colors).
- 64k Colors on XGA panels.
- Simultaneous CRT/Flat Panel operation

Display Enhancements

- 24 Bit Integrated RAMDAC with Gamma Correction.

- 24 bit TFT panel support.
- Hardware expansion for low-resolution display mode compensation to panels
- Virtual Screen Panning Support.
- Integrated Dual Clock Synthesizer.
- VESA DDCI and DDC2b.
- Enhanced VESA VAFC Input Port.

2.3.2 Pin Diagram

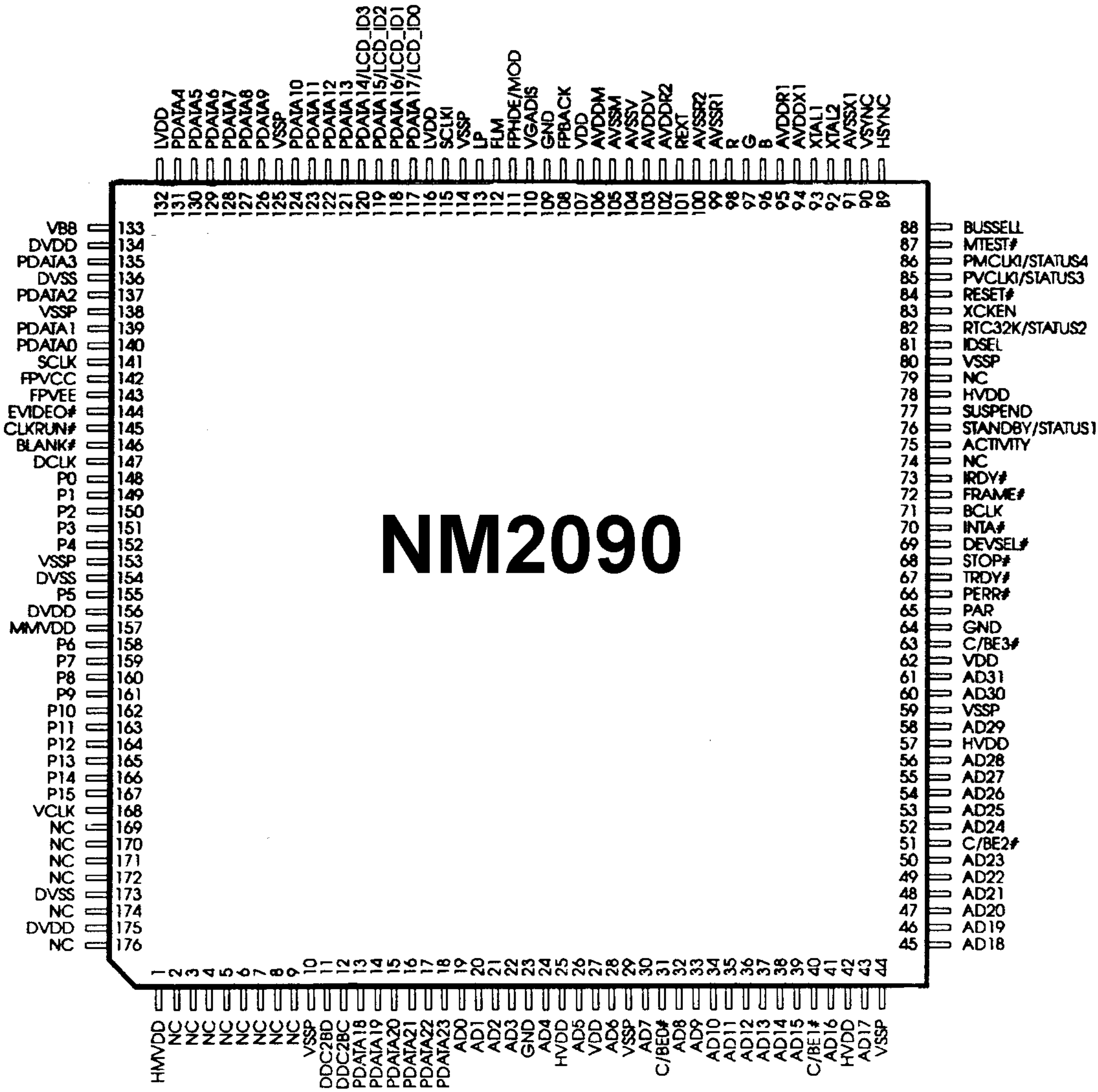


Figure 2-8 NMG2090 Pin Diagram

2.3.3 Pin Description

Conventions used in the pin description types:

Table 2-5 NMG2090 Pin Description Conventions

Item	Description	Item	Description
I	Input into NMG2	T/S	Tri-state during un-driven state
O	Output from NMG2	S/T/S	Before becoming tri-state the pin will be driven inactive
I/O	Input and Output to/from NMG2	O/D	Open-drain type output

The following table lists the pin descriptions.

Table 2-6 NMG2090 Pin Descriptions

Pin Name	Type	Pin No.	Descriptions
PCI Interface			
AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0	I/O	61 60 58 56 55 54 53 52 50 49 48 47 46 45 43 41 39 38 37 36 35 34 33 32 30 28 26 24 22 21 20 19	**Multiplexed Address and Data 31:0** These multiplexed and bi-directional pins are used to transfer address and data on the PCI bus. The bus master will drive the 32-bit physical address during address phase and data during data phase for write cycles. NM2090will drive the data bus during data phase for read cycles.

Table 2-6 NMG2090 Pin Descriptions (continued)

Pin Name	Type	Pin No.	Descriptions
PCI Interface (continued)			
C/BE3# C/BE2 C/BE1 C/BE0	I	63 51 40 31	**Multiplexed Command and Byte Enable** These multiplexed pins provide the command during address phase and byte enable(s) during data phase to the NMG2
FRAME#	I	72	**Frame** This active-low signal is driven by the bus master to indicate the beginning and duration of an access.
PAR	I/O	65	**Parity Even** parity across AD31 :0 & C/BE3:0# is driven by the bus master during address and write data phases and driven by NM2090during read data phases
IRDY#	I	73	**Initiator Ready** This active low signal indicates the bus master's ability to complete the current data phase of the transaction. During a write cycle, IDRY# indicates that valid data is present on AD31 :00 during a read cycle it indicates the master is prepared to accept data. Wait states will be inserted until both IRDY# and TRDY# are asserted together.
TRDY#	O S/T/S	67	**Target Ready** This active low signal indicates NMG2's ability to complete the current data phase of the transaction. During a read cycle TRDY# indicates that valid data is present on AD 31:00. During a write, it indicates NM2090is prepared to accept data. Wait states will be inserted until both TRDY# & IRDY# are asserted together.
STOP#	O S/T/S	68	**Stop** This active low signal indicates that NM2090is requesting the master to terminate at the end of current transaction
DEVSEL#	O S/T/S	69	**Device Select** This active low signal indicates that NM2090has decoded its address as the target of the current access.
IDSEL	I	81	**Initialization Device Select** This is selected during configuration read and write transactions.
BCLK	I	71	**Bus Clock** This input provides the timing for all transactions on PCL bus.
RESET#	I	84	**Reset** This active-low input is used to initialize NMG2.
INTA#	O O/D	70	**Interrupt request A** This active low “level sensitive" output indicates an interrupt request.

Table 2-6 NMG2090 Pin Descriptions (continued)

Pin Name	Type	Pin No.	Descriptions
VL Interface			
A23 A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2	I	18 17 16 15 14 13 12 11 9 8 7 6 5 4 3 2 176 174 172 171 170 169	**Address** These signals provide the physical memory or I/O address to NMG2.

Table 2-6 NMG2090 Pin Descriptions (continued)

Pin Name	Type	Pin No.	Descriptions
VL Interface (continued)			
D31 D30 D29 D28 D27 D26 D25 D24 D23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	I/O S/T/S	61 60 58 56 55 54 53 52 50 49 48 47 46 45 43 41 39 38 37 36 35 34 33 32 30 28 26 24 22 21 20 19	**Data** These bi-directional 32-bit data bus is used to transfer data during memory and I/O cycle.
BE3# BE2# BE1# BE0#	I	63 51 40 31	**Byte Enable** These active low byte enables indicate which bytes of the 32 bit data path are valid.
ADS#	I	72	**Address Strobe** This active low input indicates the start of a local bus cycle.
M/IO#	I	65	**Memory/IO** This input indicates the memory or I/O access currently executing on .he local bus. High level of M/IO# indicates a memory cycle and a low level indicates an I/O cycle.
W/R#	I	74	**Write/Read** This input indicates the write or read access currently executing on the local bus. High level of W/R# indicates a write cycle and a low level indicates read cycle.

Table 2-6 NMG2090 Pin Descriptions (continued)

Pin Name	Type	Pin No.	Descriptions
VL Interface (continued)			
BLAST#	I	66	**Burst Last** This input indicates the completion of a burst cycle.
RESET#	I	84	**Reset** This active low signal initializes the NM2090to a known state.
LCLK	I	71	**Local Clock** This is a 1X clock with the same phase as 486 type CPU.
RDYRTN#	I	73	**Ready Return** This input establishes a handshake between the VESA-VL bus master and NMG2. It is used by the local bus controller to generate LRDY#.
LDEV#	O S/T/S	69	**Local Device** This active Low output indicates that the NM2090will respond to the current cycle.
LRDY#	O S/T/S	68	**Local Ready** This active low output is used to terminate the claimed cycle.
BRDY#	O S/T/S	67	**Burst Ready** This active low output terminates the current active burst cycle.
INTR# /A24	O-o/d I	70	**Interrupt Request / Address 24** This active low output indicates as interrupt to CPU/ Address bit 24.(GR12 bit 0 enables/disables the Address 24 decoding).
VID2# /A26	I	79	**Low Address Decode/Address 26** This input signal is used as upper address decode during memory cycles. It is decoded from A31-A24 to select low meg address space. For a value of zero for the addresses A31-A24 VID2 should go low. /Address bit 26 (GR12 bit 2 enables/disables the Address 26 decoding).
IDSEL#, /A27	I	81	**High Address Decode** This input signal is used as upper address decode during memory cycles active low signal is the decode to support accesses to the linear memory and memory mapped IO ports/Address bit 27(GR12 bit 2 enables/disables the Address 27 decoding).
Clock Interface			
XTAL1	I	93	**Crystal Input** This is the X1 pin of the on-chip oscillator for crystal use. This pin can also be used to feed the 14.31818 MHz from an external clock source.
XTAL2	O	92	**Crystal Output** This pin is used for the 14.31818 MHz clock internally to NM2090chip when a crystal oscillator is connected between this pin and pin 93.

Table 2-6 NMG2090 Pin Descriptions (continued)

Pin Name	Type	Pin No.	Descriptions
Clock Interface (continued)			
XCKEN.	I	83	**External Clock Enable** This pin is used to select between internally synthesized clocks or externally supplied clocks. A low level on the pin selects internal mode and a high level selects external mode. In the external clock mode, the internal clock synthesizers will be disabled completely. Both PVCLK and PMCLK pins should be driven with the desired clock rates in external mode. This pin should be driven all the time during normal operation
PMCLKI / STATUS4	I/O T/S	86	**Memory Clock** This pin is used for feeding external memory clock and observing internal memory clock. When in internal clock mode (XCKEN = 0), the internal memory clock can be brought out using this pin. When in external clock mode (XCKEN = 1), PMCLKI should be driven from an external memory clock source / General purpose Status bit 4, can be read from reg CR27 bit 1. GR17 bit 0 defines the function of this pin
PVCLKI / STATUS3	I/O T/S	.85	**Video Clock** This pin is used for feeding external video clock and observing internal video clock. When in internal clock mode (XCKEN = O), the internal video clock can be brought out using this pin. When in external clock mode (XCKEN = 1),PVCLKI should be driven from an external video clock source. /General purpose Status bit 3, can be read from reg CR27 bit2. GR17 bit 1 defines the function of this pin.
Panel Interface			
FLM	O	112	First Line Marker This signal indicates start of a frame. For STN panels this pin is connected to FLM pin. For TFT panels this pin is connected to the VSYNC pin.
LP	O	113	**Line Pulse** This signal indicates start of a line. For STN panels this pin is connected to the CP1 pin. For TFT Panels, this pin is connected to the HSYNC pin
SCLK	O	141	**Shift Clock** This signal is used to drive the panel shift clock. Some panel manufacturers call this CP2.
SCLKI	O	115	**Shift Clocki** This signal is used to drive the panel shift clock. This clock is used for panels which use two clocks, one for the upper panel and the other for the lower panel.
FPHDE / MOD	O	111	**Panel horizontal Display Enable/MOD** this signal indicates the horizontal display time to the panels. For some panels it is used to drive the shift clock enable pin. This pin can also be configured to drive FPHDE for certain types of TFT panels which require separate horizontal display time indicator. **Modulation** This signal is used to drive the panel MOD or AC input

Table 2-6 NMG2090 Pin Descriptions (continued)

Pin Name	Type	Pin No.	Descriptions
Panel Interface (continued)			
FPVCC	O	142	**Flat Panel VCC** This is used to control the logic power to the panels.
FPVEE	O	143	**Flat Panel VEE** This is used to control the bias power to the panels
FPBACK	O	108	**Flat Panel Backlight** This is used to control the backlight power to the panels
PDATA23 PDATA22 PDATA21 PDATA20 PDATA19 PDATA18 PDATA17/LCD-ID0 PDATA16/LCD-ID1 PDATA15/LCD-ID2 PDATA14/LCD-ID3 PDATA13 PDATA12 PDATA11 PDATA10 PDATA9 PDATA8 PDATA7 PDATA6 PDATA5 PDATA4 PDATA3 PDATA2 PDATA1 PDATA0	O I/O I/O I/O I/O	18 17 16 15 14 13 117 118 119 120 121 122 123 124 126 127 128 129 130 131 135 137 139 140	**Panel Data** These pins are used to provide the data interface to different kinds o' panels. The following table shows the functions of these pins based on the selected panel type. PDATA23 thru PDATA18 pin are not available in VL-Bus mode, these pins are used for A18 thru A23. **LCD_ID [3..0]** pins are general purpose read only bits which can be used for panel identification. During RESET# these LCD_ID pins are inputs. The state of these bits are reflected in register CR2Eh bits3:0.The state of these bit can also be sampled anytime on-the-fly through register GR17 bit-3.1nternally these pins are pulled-up recommended external pull down resistor value is 47k ohm.
CRT Interface			
VSYNC	O T/S	90	**CRT Vertical Sync** This output is the vertical T/S synchronization pulse for the CRT monitor.
HSYNC	O T/S	89	**CRT Horizontal sync** This output is the horizontal T/S synchronization pulse for the CRT monitor.
R	O (Analog)	98	**RED** This DAC analog output drives the CRT interface.
G	O (Analog)	97	**GREEN** This DAC analog output drives the CRT interface.
B	O (Analog)	96	**BLUE** This DAC analog output drives the CRT interface.

REXT	I (Analog)	101	**DAC Current Reference** This pin is used as a current reference by the internal DAC. Please refer to the NM2090system schematics for the external circuit

Table 2-6 NMG2090 Pin Descriptions (continued)

Pin Name	Type	Pin No.	Descriptions
Power Management			
Standby / Status1	I/O	76	**Standby/Status1** The direction of the pin is controlled by GR18 bit 3. In output mode, this pin indicates the state of standby mode. The state of this pin is reflected in reg CR25 bit 5 and be used as a status pin.
Suspend	I/O	77	**Suspend** This pin can be configured as control Suspend input or status Suspend output. The active high input mode is used for controlling hardware Suspend. When asserted NM2090is forced into suspend mode where all the inputs are disabled and chip goes into the low power mode. NM2090will come out of suspend only by de-asserting this pin. During output mode, this pin will indicate the software
Activitv / A25	I/O	75	**Activity/Address 25** The direction of this pin is controlled by GR1C bit 7. This pin when in input mode and asserted indicates the system activity. A high on this pin can be used to reset internal timers. When in output mode it will indicate chip activity to the system / Address line 25 in VL-Bus mode. (GR12 bit 1 enables/disables the Address 25 decoding).
RTC32K / Status2	I/O	82	**Real Time Clock 32KhzlStatus2** This pin is used to feed 32 kHz from an external source. It is used to generate the refresh timing for the internal display memory during Standby and software Suspend modes. 14 MHz can be used to generate the memory refresh timing in above modes. General purpose Status bit 3, can be read from reg CR27 bit 0.
VAFC Interface			
P15 P14 P13 P12 P11 P10 P9 P8	I	167 166 165 164 163 162 161 160	**Pixel Data/Status 15:8** VAFC pixel data input pins, These pins are only used in 16-bit VAFC modes. These data pins connect to NM2090from the VAFC compatible interface.
P7 P6 P5 P4 P3 P2 P1 P0	I/O	159 158 155 152 151 150 149 148	**Pixel Data 7:0** VAFC pixel data bi-directional pins. The direction of these pins are controlled by ENVIDEO#. These data pins connect to NM2090from the VAFC compatible interface.
EVIDEO#	I	144	**Enable External Video Data** This is an active low signal driven by the video system to drive P15-P0 into NM2090chip. Video system should provide a pull-up on this signal. If driven inactive, NM2090will drive P7-P0 lines with

Table 2-6 NMG2090 Pin Descriptions (continued)

Pin Name	Type	Pin No.	Descriptions
VAFC Interface (continued)			
VCLK	I	168	**Video Clock** Pixel' clock driven from the video system to NM2090chip. It's used as a reference to the data and other line
DCLK	O	147	**Dot lock** This is the reference clock driven by NM2090to the video system
BLANK#	O	146	**BLANK#** This active low output indicates that NM2090is currently in the blanked region
VSYNC	O	90	**Vertical SYNC** NM2090will drive the vertical sync signal to the video system on this pin. The polarity of the vertical sync will depend on the VGA mode selected.
HSYNC	O	89	**Horizontal SYNC** NM2090will drive the horizontal sync signal to the video system on this pin. The polarity of the horizontal sync will depend on the VGA mode selected.
Miscellaneous Pins			
MTEST#	I	87	**Memory Test** This active low signal is used for internal memory testing. This should be tied high for normal system operation.
BUSSEL	I	88	**Bus Select** This pin is used to define the host bus interface type. 1 = VESA-VL bus 0 = PCI bus
CLKRUN#	I/O	145	**Clockrun** The master device will control this signal to the NMG2, according to the Mobile computing PCI design guide. If this signal is sampled high by the NM2090and the PCI clock related functions are not completed then it will drive this signal low to request the Central Clock Resource for the continuation of the PCI clock. This function can be Enabled/Disabled through reg GR12 bit 4.
DDC2BD	I/O	11	DDC Data pin
DDC2BC	I/O	12	DDC Clock pin
Power Pins			
VSSP	10, 29, 44, 59, 80, 114, 125, 138		Host bus interface ground
GND	123, 64, 109		Logic ground
DVSS	136, 154, 173		DRAM ground
VSSP	|153		VAFC interface ground
AVSSM	105		Analog ground for MCLK synthesizer
AVSSV	104		Analog ground for MCLK synthesizer
AVSSR1	99		Analog ground for VCLK synthesizer
AVSSR2	100		Analog ground for DAC current reference

Table 2-6 NMG2090 Pin Descriptions (continued)

Pin Name	Type	Pin No.	Descriptions
Power Pins (continued)			
AVSSX1	91		Analog ground for crystal oscillator
HVDD	25,42,57,78		Host bus interface VDD. (+5v or +3v) Includes the PCI, VL, CRT, Power Management, External clock pins (PMCLKI and PVCLKI) and Miscellaneous pins.
VDD	27,62.107		Logic VDD(+3V only)
DVDD	134,156,175		DRAM VDD(+3V only)
LVDD	116,132		Panel VDD (+5v or +3v)

2.4 Rockwell RCV288Aci/SVD Modem Chipset

The Rockwell RC288ACi/SVD integrated data/fax/voice/SVD modem device set supports V.34 data, V.17 fax, voice/audio, digital simultaneous voice and data (DSVD), and full-duplex speakerphone (FDSP) operation over a dial-up telephone line. Models supporting AutoSync and world class are also available.

The modem device set consists of an L39 8-bit microcomputer (MCU) packaged in a 100-pin POFP (R6723), an RCV288DPi V.34 modem data pump (MDP) packaged in a 68-pin PLCC (R6682), and a DigiTalk™ coprocessor (DTP) packaged in a 100-pin PQFP (R6693).

As a data modem, the modem operates at line speeds to 28800 bps. Error correction (V.42/MNP 2-4) and data compression (V.42 bis/MNP 5) maximize data transfer integrity and boost average data throughput up to 115.2 kbps. Non-error-correcting mode is also supported.

The modem performs error correction and data compression (ECC) in the modem using 32k bytes of external RAM. ECC increases data throughput typically by a factor of four.

As a fax modem, the modem supports Group 3 send and receive rates up to 14400 bps and supports T.30 protocol.

In voice mode, enhanced ADPCM coding and decoding supports efficient digital storage of voice using 2-bit or 4-bit compression and decompression at 7200 bps. Voice mode also supports business audio and the Integrated Communications System (ICS) program. These features support applications such as digital answering machine, voice annotation, and audio file play/record.

In DSVD mode, the DigiTalk coprocessor (DTP) provides advanced speech compression technology for use in digital simultaneous voice and data (Digital SVD or DSVD) systems. DSVD handset echo cancellation supports handset use through a hybrid. Half-duplex speakerphone (HDSP) or headset use is also supported in DSVD mode. Full-duplex speakerphone (FDSP) mode also uses the DigiTalk coprocessor.

Features

- Data modem throughput up to 115.2 kbps
  - V.34, V.FC, V.32 bis, V.32, V.22 bis, V.22A/B, V.23, and V.21; Bell 212A and 103
  - V.42 LAPM and MNP 2-4 error correction
  - V.42 bis and MNP 5 data compression
  - MNP 10 data throughput enhancement
  - MNP 10EC™ enhanced cellular performance
  - Hayes AutoSync (option)
- Fax modem send and receive rates up to 14400 bps
  - V.33, V.17, V.29, V.27 ter, and V.21 channel 2

- Voice mode
  - Enhanced ADPCM compression/decompression
  - Tone detection/generation and call discrimination
  - Concurrent DTMF detection
- Business audio mode using 8-bit monophonic audio data encoding at 11.025 kHz or 7200 Hz
- VoiceView alternating voice and data (AVD)
- Simultaneous voice and data over a telephone line using DSVD-compatible modems
- DSVD 8.5 kbps voice coder/decoder (codec)
  - Robust DSVD timing recovery
  - Handset echo cancellation
  - Voice/silence coding
  - Decoder adaptive postfilter
- Full-duplex speakerphone
  - Acoustic and line echo cancellation
  - Selectable microphone AGC and muting
  - Speaker volume control and muting
  - Auto fallback to pseudo duplex
- World-class operation (option)
  - Call progress, blacklisting, multiple country support
- Communication software compatible AT command sets
- NVRAM directory and stored profiles
- Built-in DTE interfaces with speed up to 115.2 kbps
  - Parallel 16550A UART -compatible interface
  - Serial CCITT V.24 (ElAmA-232-E)
- Supports Rockwell PnP ISA Bus Interface Device
- Supports Serial PnP interface per Plug and Play External COM Device Specification, Rev 1.00
- Flow control and speed buffering
- Automatic format/speed sensing to 115.2 kbps
- Serial async data; parallel async data
- Auto dial and auto answer; tone and pulse dialing
- Caller ID and distinctive ring detect

- Device packages
  - MCU (R6723): 100-pin PQFP
  - MDP (R6684) 68-pin PLCC
  - DTP (R6693): 100-pin PQFP
- +5V operation
- Power use (typ.): Operating = 1.75 W; Sleep = 220 mW

Architecture Block Diagram

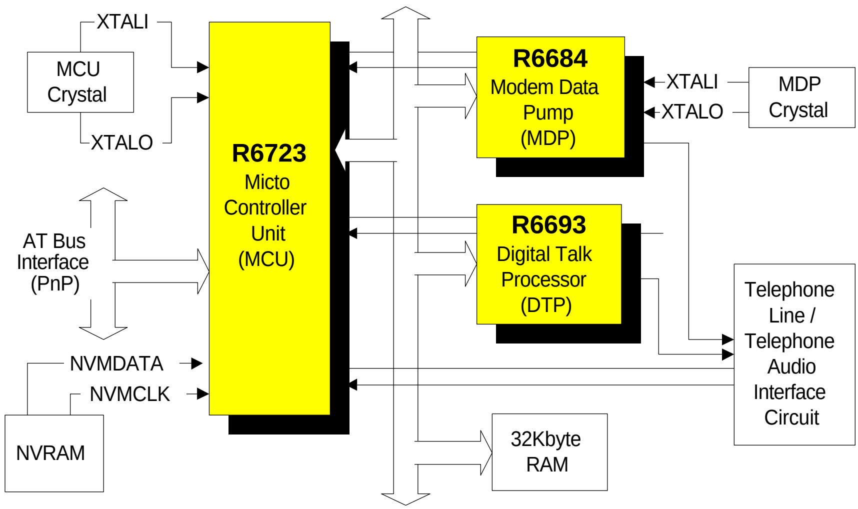


Figure 2-9 RCV288Aci/SVD Architecture Block Diagram

Signal Types Annotation

Table 2-7 RCV288Aci/SVD Signal Type Annotation

Item	Description
DI	Device interconnect.
OA	TTL output with tri-state
OB	TTL output with tri-state
OC	Open drain output
OD	Relay driver output
OE	OE outputs provide oscillator feedback when operating with an external crystal.
IA	TTL input
IB	TTL input with pull-up
IC	CMOS input with pull-up
ID	Reset signal
IE	IE inputs are centered approximately 2.5V and swing 1.5Vpeak in each direction.

Table 2-7 RCV288Aci/SVD Signal Type Annotation (continued)

Item	Description
I(DA)	Analog input, input impedance > 70KΩ, maximum AC input voltage range is 1.7Vp-p, and reference voltage is +2.5Vdc.
O(DD)	Analog output, maximum load is 300Ω, output impedance > 10Ω, AC output voltage range is 2.2Vp-p, DC offset voltage is ±200mV, and reference voltage is +2.5Vdc.
O(DF)	Analog output, maximum load is 300Ω, output impedance > 10Ω, AC output voltage range is 2.2Vp-p, DC offset voltage is ±20mV, and reference voltage is +2.5Vdc.

2.4.1 R6723-12 MCU (Microcomputer) Chip

Pin Diagram

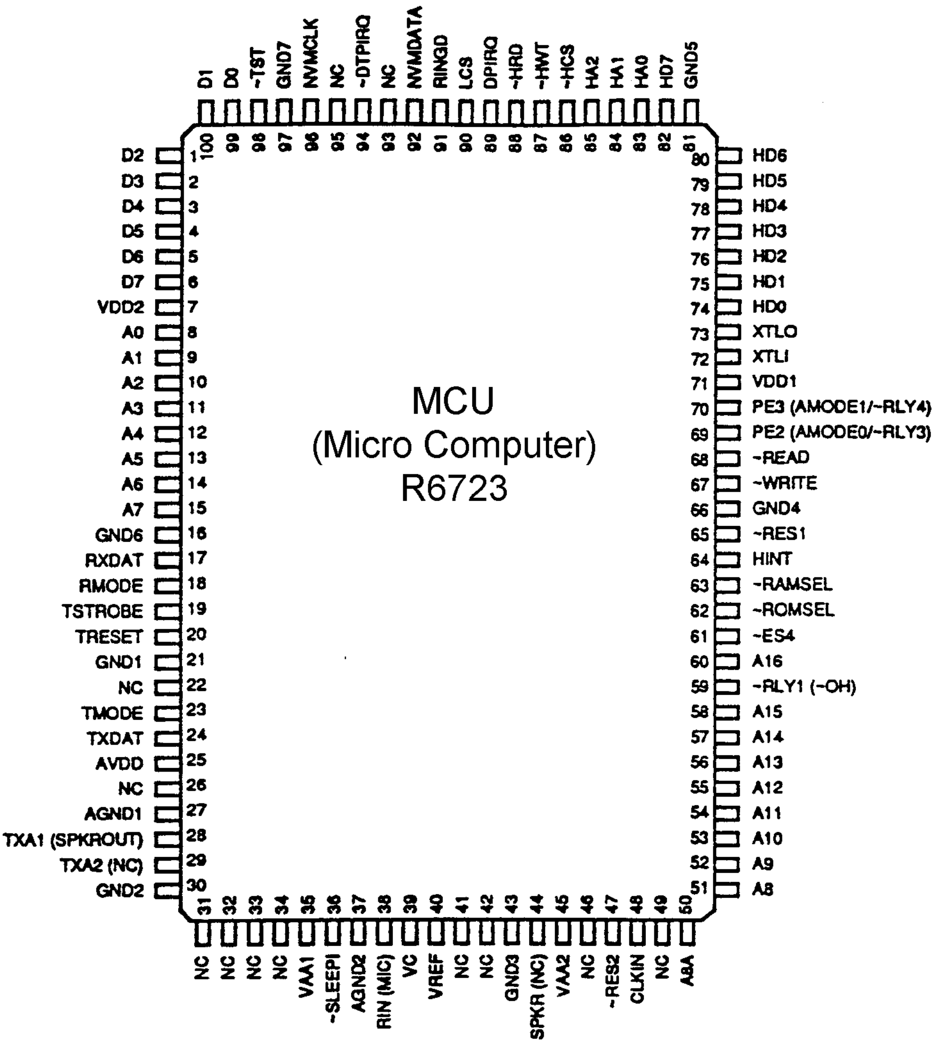


Figure 2-10 R6723-12 Pin Diagram

Pin Descriptions

Table 2-8 R6723-12 Pin Descriptions

Pin Name	Pin Type	Pin No.	Descriptions
XTLI XTLO	IE OE	72 73	**Crystal/Clock In and Crystal Out.** Connect to an external 14.7456 MHz crystal circuit.
-RES1 -RES2	IC IA	65 47	**MCU Reset.** The active low -RESn input resets the MCU logic, and restores the saved configuration from NVRAM or returns the modem to the factory default values. if NVRAM is not present, -Resin low holds the modem in the reset state; -RESET going high releases the modem from the reset state. After application of +5V, -RESn must be held low for at least 15 ms after the +5V power reaches operating range. The modem device set is ready to use 25 ms after the low-to-high transition of -RESn.
DPIRQ	IA	89	**MDP Interrupt Request.** Connect to the MDP IRQ output
VDD1-VDD2	PWR	71 7	**+ 5V Digital Supply Voltage.** Connect to +5V.
AVDD(P5VD), VAA1(P5VT) VAA2(PSVR)	PWR	25 35 45	**+5V Analog Supply Voltage.** Connect to VCC through a decoupling circuit.
GND4-GND7	GND	66 81 16 97	**Digital Ground.** Connected digital ground.
GND1-GND3	GND	21 30 43	**Analog Ground.** Connect to analog ground.
-STPMODE	IA		**Stop Mode.** Connect to VCC through 10KΩ.
-TST	IA	98	**Test mode.** -TST controls MCU access to internal ROM.(High= enables internal ROM; This pin has an internal pull-up. Connect -TST to GND.
NVRAM Interface			
NVMCLK	OA	96	**NVRAM clock.** NVMCLK output high enables the NVRAM.
NVMDATA	IA/OA	92	**NVRAM Data.** The NVMDATA pin supplies a serial data interface to the NVRAM.
External Memory Bus Interface			
A0-A15	OA	8:15, 51:58	**Address Line 0-15.** A0~A15 are the external memory bus address lines.
A16	OA	60	**Address Line 16.** A16 is a bank select line.
D0-D7	IA/OA	99:100, 1:6	**Data line 0-7.** D0-D7 an the external memory bus data lines.
-READ	OA	68	**Read Enable.** -READ output low enables data transfer from the selected device to the DSD7 lines.

Table 2-8 R6723-12 Pin Descriptions (continued)

Pin Name	Pin Type	Pin No.	Descriptions
External Memory Bus Interface (continued)			
-WRITE	OA	67	**Write Enable.** WRITE output low enables data transfer from the D0-D7 lines to the selected device.
-RAMSEL	OA	63	**RAM Select.** -RAMSEL output low selects the external 32kbyte RAM.
-ROMSEL	OA	62	**ROM Select.** -ROMSEL output low selects an external 128k-byte ROM or flash ROM.
-ES4	OA	61	**ES4 Select.** The -ES4 output and address line A5 are used by external logic to generate the MDP chip select (-DPSEL = -ES4 low and A5 low) and the DTP chip select (-SPSEL = -ES4 low and A5 high).
Host Interface: The parallel interface emulates a 16S50A UART-compatible interface.			
HA0-HA2	IA	83:85	**Host Bus Address Lines 0-2.** During a host read or write operation with -HCS low, HA0-HA2 select an internal MCU 16550A-compatible register.
HD0-HD7	IA/OB	74:80,82	**Host Bus Data Lines 0-7.** HD0-HD7 are comprised of eight three-state input/output lines providing bidirectional communication between the host and the MCU Data, control words, and status information are transferred over HD0-HD7
-HCS	IA	86	**Host Bus Chip Select.** -HCS input low enables MCU host bus interface.
-HRD	IA	88	**Host Bus Read.** -HRD is an active low, read control input. When -HCS is low, -HRD low allows the host to read status information or data from a selected MCU register.
-HWT	IA	87	**Host Bus Write.** -HWT is an active low, write control input. When -HCS is low, -HWT low allows the host to write data or control words into a selected MCU register
HINT	OA	64	**Host Bus Interrupt.** HINT output is set high when the receiver error flag, received data available, transmitter holding register empty, or modem status interrupt is asserted HINT is reset low upon the appropriate interrupt service or master reset operation.
Telephone Line Interface			
-RLY1 (-OH) (PE0)	OA	59	**Relay 1 Control (-OH).** MCU port PE0 is assigned to the -RLY1 output signal. The active low -RLY1 output can be used to control the normally open off-hook relay. The -PULSE function is also provided on this line for single -OH/-PULSE relay application.
-RLY3 (PE2)	OA	69	**Relay 3 Control (-MUTE).** When MCU port PE2 is enabled as a relay driver, the active low -RLY3 output can be used to control the normally open mute relay (W-class). This port can also be used to drive the AMODE0 mux control line.

Table 2-8 R6723-12 Pin Descriptions (continued)

Pin Name	Pin Type	Pin No.	Descriptions
Telephone Line Interface (continued)			
-RLY4 (PE3)	OA	70	**Relay 4 Control (-EARTH).** When MCU port PE3 is enabled as a relay driver, the active low -RLY4 output can be used to control the normally open earthing relay (W-class). This port can also be used to drive the AMODE1 mux control line.
LCS	IA	90	**Loop Current Sense.** LCS is an active high input that indicates a handset off-hook status
RINGD	IA	91	**Ring Frequency.** A rising edge on the RINGD input initiates an internal ring frequency measurement. The RINGD input from an external ring detect circuit is monitored to determine when to wake up from sleep mode. The RINGD input is typically connected to the output of an optoisolator or equivalent. The idle state (no ringing) output of the ring detect circuit should be low.
Audio Interface			
SPKROUT (TXA1) NC (TXA2)	O(DF)	28 29	**Speaker Analog Output.** The TXA1 and TXA2 outputs are differential outputs 180 degrees out of phase with each other. The output characteristics are the same as a 1458 type OP amp. TXA1 is used as a single ended output (SPKROUT) to an external amplifier in the audio interface circuit. TXA2 is not connected (open).
MIC (RIN)	I(DA)	38	**Microphone Analog Input.** MIC (RIN) is a single ended microphone input from the audio interface circuit. The input impedance is > 7014Ω.
DTP Reference Signals and Device Interconnect			
VC	DI	39	**Low Voltage Reference.** Connect to analog ground through a 10 pF (polarized, + terminal to VC) and a 0.1 pF (ceramic) in parallel.
VREF	DI	40	**High Voltage Reference.** Connect to VC through 10 pF (polarized, + terminal to VREF) and 0.1 pF (ceramic) in parallel.
-SLEEPI	DI	36	**Sleep.** Connect to DTP: -SLEEPO.
RXDAT	DI	17	**Receive Data In.** Connect to DTP: SR41N.
TXDAT	DI	24	**Transmit Data In.** Connect to DTP: SR30UT.
TMODE	DI	23	**Transmitter Mode.** Connect to MCU RMODE and to DTP: TMODE, RMODE and SR3OUT.
RMODE	DI	18	**Receiver Mode.** Connect to MCU TMODE and to DTP: TMODE, RMODE and SR1IO.
CLKIN.	DI	48	**CLKIN.** Connect to DTP IACLK.

2.4.2 R6684-17 MDP (Modem Data Pump) Chip

Pin Diagram

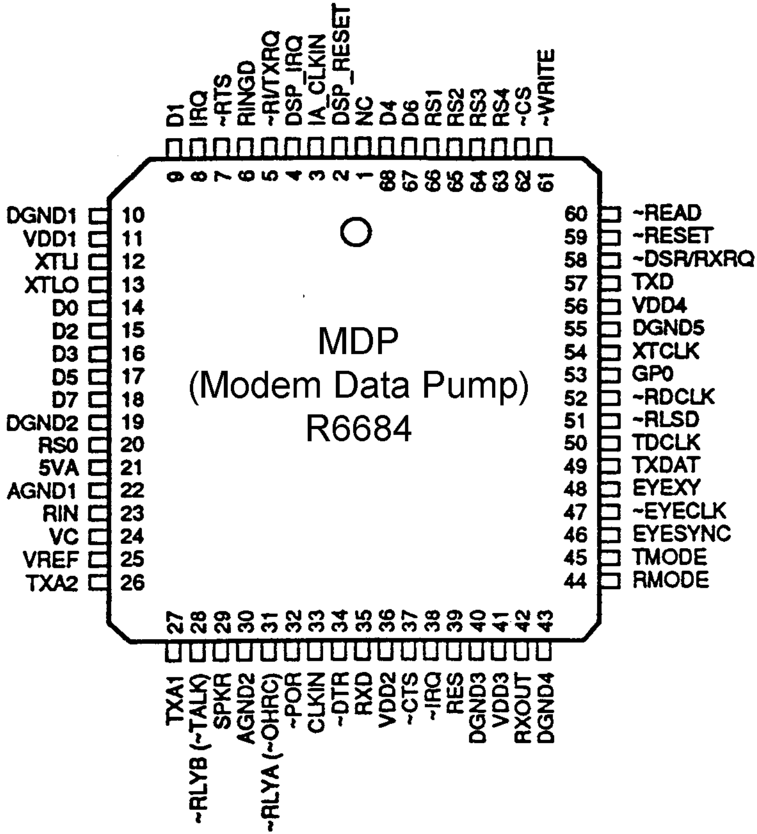


Figure 2-11 R6684-17 Pin Diagram

Pin Descriptions

Table 2-9 R6684-17 Pin Descriptions (MDP)

Pin Name	Pin Type	Pin No.	Descriptions
XTLI XTLO	I O	12 13	**Crystal In and Crystal Out.** Connect to an external 40.32 MHz crystal circuit or square wave generator/sine wave oscillator circuit.
-RESET	IA	59	**Reset.** -RESET low holds the MDP in the reset state. -RESET going high releases the modem from the reset state and initiates normal operation using power turn-on (default) values. -RESET must be held low for at least 3 us. The modem is ready to use 400 ms after the low-to-high transition of -RESET
VDD1-VDD3	PWR	11,36.41	**+5V Digital Supply Voltage.** Connect to +5V.
+5VA	PWR	21	**+5V Analog Supply Voltage.** Connect to VCC through a decoupling circuit
DGND1 - DGND5	GND	10, 19, 40, 43, 55	**Digital Ground.** Connect to digital ground.
AGND1 - AGND2	GND	22, 30	**Analog Ground.** Connect to analog ground.
VC	DI	24	**Centerpoint Voltage.** Connect to analog ground through 10 pF (polarized, + terminal to VC) and 0.1 pF (ceramic) in parallel.
VREF	DI	25	**Voltage Reference.** Connect to VC through 10 pF (polarized, + terminal to VREF) and 0.1 pF (ceramic) in parallel.
MCU Interface			
D0-D8	IA/OB	14, 9, 15, 16, 68, 17, 67, 18	**Data Lines.** Connect to the MCU external bus D0-D7 lines, respectively.
RS0-RS4	IA	20, 66:63	**Register Select Lines.** Connect to the MCU external bus A0-A4 lines, respectively.
-READ	IA	60	**Read Enable.** Connect to MCU external bus -READ line
-WRITE	IA	61	**Write Enable.** Connect to MCU external bus -WRITE line
-CS	IA	62	**Chip Select.** Connect to -DPSEL from the MDP/DTP chip select decode logic.
IRQ	OA	8	**Interrupt Request.** Connect to MCU DPIRQ
MODEU Sterconnect			
-POR	DI	32	**Power-On-Reset.** Connect to -RESET.
DSP_RESET	DI	2	**DSP Reset.** Connect to-RES.
-RES	DI	39	**Reset.** Connect to DSP RESET.
DSP_IRQ	DI	4	**DSP Interrupt Request.** Connect to -IRQ
-IRQ	DI	38	**Interrupt Request Connect.** to DSP_IRQ

IA_CLKIN	DI	3	**IA Clock.** Connect to CLKIN.

Table 2-9 R6684-17 Pin Descriptions (MDP) (continued)

Pin Name	Pin Type	Pin No.	Descriptions
MODEU Sterconnect (continued)			
CLKIN	DI	33	**Clock.** Connect to IA_CLKIN.
RMODE	DI	44	**Receiver Mode.** Connect to TMODE.
TMODE	DI	45	**Transmitter Mode.** Connect to RMODE.DTE INTERFACE
TXD	IA	57	**Transmitted Data.** Not used; pull up to VCC through 10k n
RXD	OA	35	**Received Data.** Not used; leave open
TDCLK	OA	50	**Transmit Data Clock.** Not used; leave open.
XTCLK	IA	54	**External Transmit Clock.** Not used; leave open.
-RDCLK	OA	52	**Receive Data Clock.** Not used; leave open.
-RLSD	OA	51	**Received Line Signal Detector.** Not used, leave open.
-RTS	IA	7	**Request to Send.** Not used; pull up to VCC through 10kΩ
-DTR	IA	34	**Data Terminal Ready.** Not used; pull up to VCC through 10k n.
-CTS	OA	37	**Clear to Send.** Not used; leave open
-DSR	OA	58	**Data Set Ready.** Not used; leave open.
Telephone Line Interface Signals			
TXA1 TXA2 (NC)	O(DF)	27 26	**Transmit Analog 1 and 2.** The TXA1 and TXA2 outputs are differential outputs 180 degrees out of phase with each other. Each output can drive a 300Ω load. TXA2 is not used
RIN	I(DA)	23	**Receive Analog.** RIN is a single-ended receive data input from the telephone line/audio interface circuit
RINGD	IA	6	**Ring Detect.** The RINGD input is monitored for pulses in the range of 15 Hz to 68 Hz. The frequency detection range may be changed by the host in DSP RAM. The circuit driving RINGD should be a 4N35 optoisolator or equivalent. The circuit driving RINGD should not respond to momentary bursts of ringing less than 125 ms in duration, or less than 40 VRMS (15 Hz to 68 Hz) across TIP and RING. Detected ring signals are reflected on the -RI output signal as well as the RI bit
-RLYA (-OHRC)	OD	31	**Relay A (Caller ID) Control.** The MDP -RLYA output is connected to the Caller ID relay (DPDT). When Caller ID is enabled, the modem doses the Off-hook relay and asserts this output to switch the Caller ID in order to detect Caller ID information between the first and second rings. The -RLYA output can directly drive a +5V reed relay coil with a minimum resistance of 360 ohms and having a must-operate voltage of no greater than 4.0 Vdc. A clamp diode, such as a 1 N4148, should be installed across the relay coil. An external transistor, such as an MPSA20, can be used to drive heavier loads (e.a., electro-mechanical relays).

Table 2-9 R6684-17 Pin Descriptions (MDP) (continued)

Pin Name	Pin Type	Pin No.	Descriptions
-RLYB (-TALK)	OD	28	**Relay B (Voice) Control.** The MDP -RLYB output is connected to the Voice relay (DPDT). In voice mode, the modem asserts the this output to switch the handset from the telephone line to a current source to power the handset so it can be used as a microphone and speaker interface to the modem. The -RLYB output can directly drive a +5V reed relay coil with a minimum resistance of 360Ω and having a must-operate voltage of no greater than 4.0 Vdc. A damp diode, such as a 1N4148, should be installed across the relay coil. An external transistor, such as an MPSA20, can be used to drive heavier loads (e.g., electro-mechanical relays).
Speaker Interface			
SPKR (MSPKR)	O(DF)	29	**Modem Speaker Analog Output.** The SPKR output reflects the received analog input signal. The SPKR is controlled by the ATMn command. The SPKR output can drive an impedance as low as 300Ω. In a typical application, the SPKR output is an input to an external LM386 audio power amplifier.
Diagnostic Signals			
EYEXY	OA	48	**Serial Eye Pattern W/Y Output.** EYEXY is a serial output containing two 15 bit diagnostic words (EYEX and EYEY) for display on the oscilloscope X axis (EYEX) and Y axis (EYEY).
-EYECLK	OA	47	**Serial Eye Pattern Clock.** -EYECLK is a 288 kHz output clock for use by the serial-to-parallel converters.
EYESYNC	OA	46	**Serial Eye Pattern Strobe.** EYESYNC is a strobe for loading the D/A converters.

2.4.3 R6693-14 DTP (DigiTalk Processor) Chip

Pin Diagram

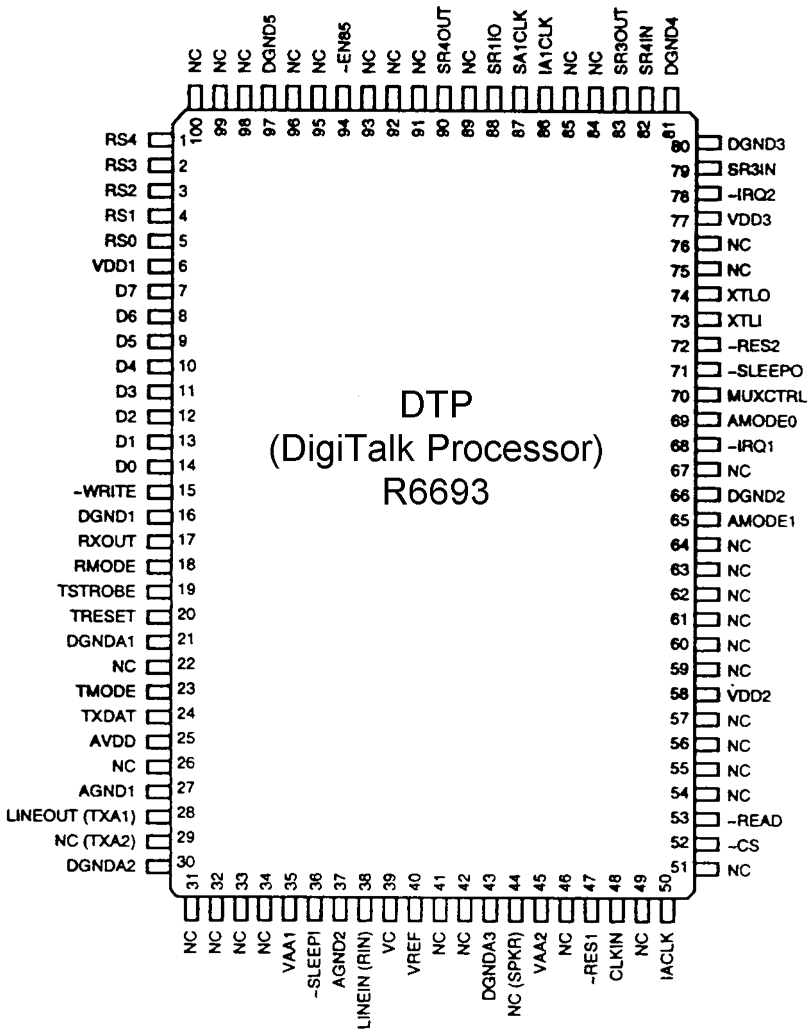


Figure 2-12 R6693-14 Pin Diagram

Pin Descriptions

Table 2-10 R6693-14 Pin Descriptions

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Pin No.</th><th>Descriptions</th></tr>
<tr><td>XTLI, XTLO</td><td>R</td><td>73, 74</td><td>Crystal In and Crystal Out. Connect to an external 49.92 MHz fundamental or third overtone crystal circuit.</td></tr>
<tr><td>-RESET</td><td>ID</td><td></td><td>Reset. After application of +5V power, -RESET must be held low for at bast 15 ms after the +5V power reaches operating range. The DTP is ready to use 25 ms after the low-to-high transition of -RESET. The reset sequence initializes the DTP interface memory to default values.</td></tr>
<tr><td>-POR</td><td>IA</td><td></td><td>Power-On-Reset. Connect to -RESET</td></tr>
<tr><td>VDD1-VDD3</td><td>PWR</td><td>6, 58, 77,</td><td>+5V Digital Supply Voltage. Connect to Vcc</td></tr>
<tr><td>AVDD, VAA1, VAA2</td><td>PWR</td><td>25, 35, 45,</td><td>+5V Analog Supply Voltage. Connect to VCC through decoupling circuit</td></tr>
<tr><td>DGND1-DGND5</td><td>GND</td><td>16, 66, 80, 81, 97</td><td>Digital Ground. Connect to digital ground.</td></tr>
<tr><td>DGNDA[1:3]
AGND[1:2]</td><td>GND</td><td>21, 30, 42, 27, 37</td><td>Analog Ground. Connect to analog ground.</td></tr>
<tr><td>D0-D7</td><td>IA/OB</td><td>14:7</td><td>Data Lines. Connect to the MCU external bus D0-D7 lines, respectively.</td></tr>
<tr><td>RS0-RS4</td><td>IA</td><td>5:1</td><td>Register Select Lines. Connect to the MCU external bus A0-A4 lines respectively.</td></tr>
<tr><td>-CS</td><td>IA</td><td>52</td><td>Chip Select. Connect to -SPSEL output from be MDP/DTP chip select decode logic.</td></tr>
<tr><td>-READ</td><td>IA</td><td>53</td><td>Read Enable. Connect to the MCU external bus -READ line.</td></tr>
<tr><td>-WRITE</td><td>IA</td><td>15</td><td>Write Enable. Connect to MCU external bus -WRITE line.</td></tr>
<tr><td>LINEOUT</td><td>O(DF)</td><td>28</td><td>Line Out Analog Output. The LINEOUT is a single-ended output to the telephone line through the hybrid circuit. The output can drive a 300Ω load.</td></tr>
<tr><td>LINEIN</td><td>I(DA)</td><td>38</td><td>Line In Analog Input. The LINEIN is a single ended input from the audio interface.</td></tr>
<tr><td>AMODE0 (SP2),
AMODE1 (SP3)</td><td>OA</td><td>69, 65</td><td>Audio Mode Select. single-ended output to the audio interface circuit, typically through a 74HC4052 analog multiplexer /demultiplexer. The modes are:
<table>
<tr><th>AMODE 1:0]</th><th>Function</th><th>Receive Input to the MDP (Y)</th><th>Transmit Output Via to the DAA (X)</th></tr>
<tr><td>00</td><td>Microphone Record</td><td>Microphone Input</td><td>TXA from MDP</td></tr>
<tr><td>01</td><td>Sound Chips</td><td>RXA from DAA</td><td>SCOUT from sound chips</td></tr>
<tr><td>10</td><td>Speakerphone</td><td>RXA from DAA</td><td>LINEOUT from DTP</td></tr>
<tr><td>11</td><td>Data/Fax/Voice/BA/ Record Conversation</td><td>PLXA from DAA</td><td>TXA from MDP</td></tr>
</table></td></tr>
<tr><td>-EN85</td><td>IA</td><td>94</td><td>Enable 85 Bus. Connect to GND</td></tr>
</table>

Table 2-10 R6693-14 Pin Descriptions (continued)

Pin Name	Pin Type	Pin No.	Descriptions
-SLEEPI	IA	36	**Sleep.** Connect to the DTP -SLEEPO pin and to MCU -SLEEPI pin
VC	DI	39	**Low Voltage Reference.** Connect to analog ground through 10 pF (polarized, + terminal to VC) and 0.1µF(ceramic) in parallel.
VREF	DI	40	**High Voltage Reference.** Connect to VC through 10 pF (polarized, + terminal to VREF) and 0.1µF (ceramic) in parallel.
SR1IO	DI	88	**SR1IO.** Connect to DTP: TMODE & RMODE, and to the MCU TMODE and RMODE pins
TMODE	DI	23	**Transmitter Mode.** Connect to DTP: SR1IO.
RMODE	DI	18	**Receiver Mode.** Connect to DTP: SR1IO.
SR31N	DI	79	**SR31N.** Connect to DTP: RXOUT
RXOUT	DI	17	**Receive Data Out.** Connect to DTP: SR31N
SR4OUT	DI	90	**SR4OUT.** Connect to DTP: TXDAT.
TXDAT	DI	24	**Transmit Data In.** Connect to DTP: SR40UT.
IACLK	DI	50	**IACLK.** Connect to DTP: CLKIN and to MCU CWN
CLKIN	DI	48	**CLKIN.** Connect to DTP: IACLK
IA1CLK	DI	86	**IA1CLK.** Connect to DTP: TSTROBE.
TSTROBE	DI	19	**Transmitter Strobe.** Connect to DTP: IA1CLK
SA1CLK	DI	87	**SA1CLK.** Connect to DTP: TRESET.
TRESET	DI	20	**Transmitter Reset.** Connect to DTP: SA1CLK
SR41N	DI	82	**SR41N.** Connect to MCU: RXDAT.
SR3OUT	DI	83	**SR3OUT.** Connect to MCU: TXDAT.

2.5 ESS1688W Sound Controller

ESS Technology has developed the ES1688W AudioDrive®, a single chip solution for adding 16-bit stereo audio and four-operator FM music synthesis to personal computers. It has integrated all the major blocks of audio in to a single chip that can be designed into a motherboard, notebook PC, add-on card, or integrated onto other peripheral cards such as VGA, LAN, I/O, etc.

The ES1688W AudioDrive can record, compress, and playback voice, sound and music with built-in mixer controls. It consists of an embedded microprocessor, 16-bit stereo A/D and D/A, 20-voice FM music synthesizer, MIDI serial port compatible with MPU401 UART mode, DMA control, and ISA bus interface logic. A DSP serial interface allows an external DSP to take over analog resources such as the D/A or A/D converters. Control of I/O address, DMA, and interrupt selection can be by jumper or by control of system software. Interface to analog inputs is extremely simple. There are stereo inputs for CD-audio, line-in, and an external music synthesis chip, and a mono microphone input to an internal pre-amp. A digital PC speaker input is converted to an analog signal with volume control and is available as an analog output signal. Address decode outputs simplify interfacing to a game port. Advanced power management features such as Suspend/Resume and partial power-down are supported.

The ES1688W AudioDrive is compatible with Sound Blaster PRO™ version 3.01 voice and music functions as documented in the Sound Blaster Series Developer Kit.

The ES1688W is pin-compatible with the ES688 AudioDrive.

2.5.1 Block Diagram

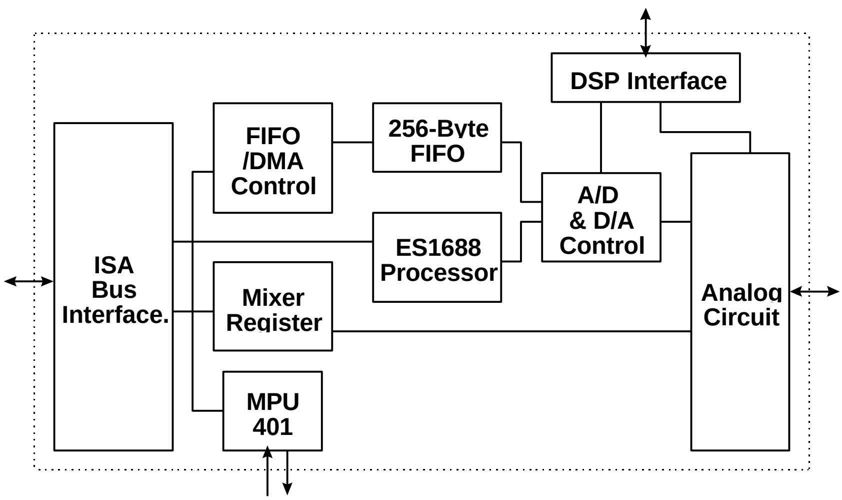


Figure 2-13 ESS1688W Block Diagram

2.5.2 Pin Diagram

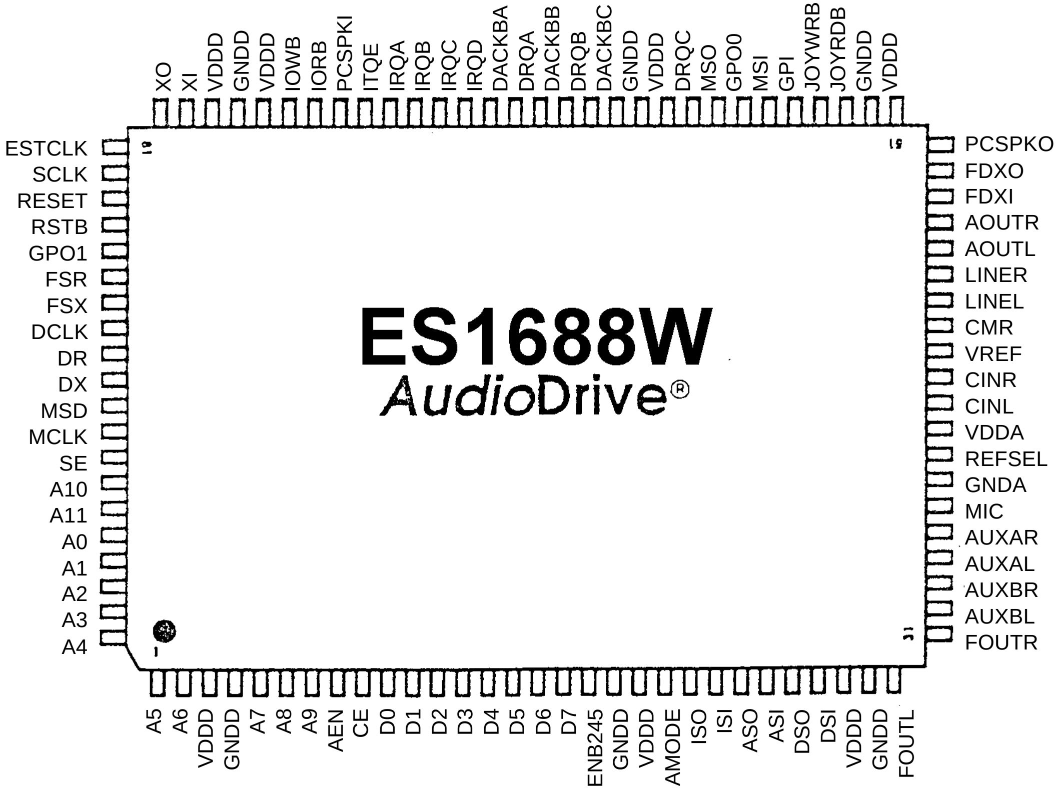


Figure 2-14 ESS1688W Pin Diagram

2.5.3 Pin Descriptions

Table 2-11 ESS1688W Pin Descriptions

Pin name	Number	I/O	Description
Digital Pins			
VDDD	3, 28, 51, *75,* 20, 60, 78	I	Digital Supply Voltage (3.0V to 5.5V)
GNDD	4, 29, 52, 76 19, 61, 77	I	Digital Ground
JOYWRB	54	O	Active low decode for joystick, write to port 201H.
JOYRDB	53	O	Active low decode for joystick, read from port 201H.
GPO0	57	O	Output that is set low by external reset and thereafter controlled by bit 0 of port 2x7H. Available to system software for power management or other applications.
GPO1	85	O	Output that is set high by external reset and thereafter controlled by bit 1 of port 2x7H. Available to system software for power management or other applications.
MSI	56	I	MIDI serial input. Schmitt trigger input with internal pull-up resistor.
MSO	58	O	MIDI serial data output.
GPI	55	I	Reserved General Purpose Input with internal pull-down. Currently no function is assigned to this pin, and any connection is acceptable.
RESET	83	I	Active high reset from ISA bus.
RSTB	84	O	Inverted RESET output.
SCLK	82	I	Clock selection input: @0: Clock from EXTCLK input@1: Clock from crystal connected to pins XI and XO
EXTCLK	81	I	14.32 MHz clock input from ISA bus. Duty cycle must be 40%-60% . No connection if SCLK = 1.
XO	79	O	Optional crystal output.
XI	80	I	Optional crystal input. No connection if SCLK=0.
CE	9	I	Input with internal pull-up. Active high chip enable. When low all IRQ outputs and DRQ outputs become high impedance, and AEN is forced high internally, thereby disabling I/O activity to/from the ESl688. Outputs FMCSB, JOYRDB, and JOYWRB become inactive high. Leave unconnected or connected to VDD for normal operation.
IORB	73	I	Active low read strobe from ISA bus.
IOWB	74	I	Active low write strobe from ISA bus.

Table 2-11   ESS1688W Pin Descriptions (continued)

Pin name	Number	I/O	Description
Digital Pins			
A0-A9	96-100, 1, 2, 5-7	I	Address inputs from ISA bus.
A10-A11	94,95	I	Address inputs from ISA bus. The ES1688W requires these pins to be low for all address decodes. These pins have an internal pulldown device enabled when input signal AMODE=0. In this case they can float (ES688 compatible designs).
AEN	8	I	Active low address enable from ISA bus.
D0-D7	10-17	I/O	Bi-directional data bus. These pins have weak pull-up devices to prevent these inputs from floating when not driven.
ENB245	18	O	Active low output when ES1688W is being read or written to. Intended to be connected to the enable control of an external 74LS245.
DS0, DS1	26, 27	I	Inputs with internal pull-down devices. These inputs select the DMA channel selected after external reset: DS1 · DS0 · DRQx/DACKBx · Recommended ISA DRO/DACK 0 · 0 · No DRQ or DACK 0 · 1 · DRQA, DACKBA · DRQ0/-DACK0 1 · 0 · DRQB, DACKBB · DRQ1/-DACK1 1 · 1 · DRQC, DACKBC · DRQ3/-DACK3 DSl=0 and DS0=0 is a special case: no DMA request or interrupt request pin is selected after external reset. Software configuration of interrupt and DMA channels are required.
IS0, IS1	22, 23	I	Inputs with internal pull-down devices. These inputs select the default interrupt request pin selected after external reset (unless DS1 =0 and DS0=0). IS1 · IS0 · IRQX · Recommended ISA IRQ 0 · 0 · IRQA · IRQ9 0 · 1 · IRQB · IRQ5 1 · 0 · IRQC · IRQ7 1 · 1 · IRQD · IRQl0
AMODE	21	I	Input pin with internal pulldown device. If this pin is low, then AS0 and ASI act as in the ES688, namely, they directly select the base address of the ESI680 I/O address bank. If this pin is high, then AS0 and ASI can be configured to select one of two software address selection techniques.

Table 2-11 ESS1688W Pin Descriptions (continued)

<table>
<tr><th>Pin name</th><th>Number</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="4">Digital Pins</td></tr>
<tr><td>AS0, AS1</td><td>24, 25</td><td>I</td><td>Inputs with internal pull-down devices. Along with AMODE, these inputs select the I/O address bank or the software address selection technique. They should be jumpered to VDDD or GNDD:
<table>
<tr><th>AMODE</th><th>ASI AS0</th><th>Function</th></tr>
<tr><td>0</td><td>00</td><td>220 base address</td></tr>
<tr><td>0</td><td>01</td><td>230 base address</td></tr>
<tr><td>0</td><td>10</td><td>240 base address</td></tr>
<tr><td>0</td><td>11</td><td>250 base address</td></tr>
<tr><td>1</td><td>00</td><td>220 base address</td></tr>
<tr><td>1</td><td>01</td><td>Read-Sequence-Key address selection.</td></tr>
<tr><td>1</td><td>10</td><td>240 base address</td></tr>
<tr><td>1</td><td>11</td><td>System-Control-Register address selection</td></tr>
</table>
Because the pulldown devices on these pins are weak, in a high noise environment there might be glitching on a floating trace running to an open option switch. In such a case either use an external pulldown resistor or a shorting block that goes to either VDDD or GNDD

Note: when AMODE=0, address inputs A10 and A11 have internal pull-down devices. When AMODE= 1, they do not.
<table>
<tr><th>AMODE</th><th>ASI AS0</th><th>Function</th></tr>
<tr><td>0</td><td>00</td><td>220 base address</td></tr>
<tr><td>0</td><td>01</td><td>230 base address</td></tr>
<tr><td>0</td><td>10</td><td>240 base address</td></tr>
<tr><td>0</td><td>11</td><td>250 base address</td></tr>
<tr><td>1</td><td>00</td><td>220 base address</td></tr>
<tr><td>1</td><td>01</td><td>Read-Sequence-Key address selection.</td></tr>
<tr><td>1</td><td>10</td><td>240 base address</td></tr>
<tr><td>1</td><td>11</td><td>System-Control-Register address selection</td></tr>
</table>
Because the pulldown devices on these pins are weak, in a high noise environment there might be glitching on a floating trace running to an open option switch. In such a case either use an external pulldown resistor or a shorting block that goes to either VDDD or GNDD

Note: when AMODE=0, address inputs A10 and A11 have internal pull-down devices. When AMODE= 1, they do not.</td></tr>
<tr><td>IRQA,B,C,D</td><td>70-67</td><td>O</td><td>Active high interrupt request to ISA bus. Unselected IRQ outputs are high impedance. IRQs are selected after external reset based on the settings of inputs IS1 and IS0 and can be reprogrammed thereafter.</td></tr>
<tr><td>IRQE</td><td>71</td><td>O</td><td>Active high interrupt request to ISA bus. Reserved for MPU401 use.</td></tr>
</table>

Table 2-11 ESS1688W Pin Descriptions (continued)

Pin name	Number	I/O	Description
Digital Pins			
DRQA, B, C	65, 63, 59	O	Active high DMA request to ISA bus. Unselected DRQ outputs are high impedance. When DMA is not active, the selected DRQ output has a pulldown device that holds the DRQ line inactive unless another device that shares the same DRQ line can source enough current to make the DRQ line active. DRQs are selected after external reset based on the settings of inputs DS1 and DS0, and can be reprogrammed thereafter.
DACKBA, B, C	66, 64, 62	I	Active low DMA acknowledge inputs from ISA bus.
PCSPKI	72	I	Normally low digital PC speaker signal input. This signal is converted to an analog signal with volume control and appears on analog output PCSPKO.
FSR	86	I	Input with internal pull-down. Frame Sync for Receive data from external DSP. Programmable for active high or active low.
FSX	8S7	I	Input with internal pull-down. Frame Sync for Transmit request from external DSP. Programmable for active high or active low.
DCLK	88	I	Input with internal pull-down. Serial data clock from external DSP. Typically 2.048 MHz.
DR	89	I	Input with internal pull-down. Data Receive pin from external DSP.
DX	90	0	Tri-state output. Data Transmit to external DSP. High impedance when not transmitting.
MSD	91	I	Input with internal pull-down. Music Serial Data from external ES689 Music Synthesizer.
MCLK	92	I	Input with internal pull-down. Music Serial Clock from external ES689 Music Synthesizer.
SE	93	I	Input with internal pull-down. Active high to enable serial mode, i.e., enables an external DSP to control analog resources of the ES1688W through the DSP serial interface.
VDDA	39	I	Analog supply voltage (4.5V to 5.5V). Should be greater than or equal to VDDD-0.3V.
GNDA	37	I	Analog Ground
MIC	36	I	Microphone input. MIC has an internal pull-up resistor to CMR.
LINE L, R	44, 45	I	Line input left, right. LINE L,R has internal pull-up resistors to CMR.
AUXA L,R	34, 35	I	Auxiliary input left, right. AUXA L,R have internal pull-up resistors to CMR. Normally intended for connection to an internal or external CD or CD-ROM analog output.
AUXB L,R	32, 33	I	Auxiliary input left right. AUXB L,R have internal pull-up resistors to CMR Normally intended for connection to an external music synthesizer or other line level source.

Table 2-11 ESS1688W Pin Descriptions (continued)

Pin name	Number	I/O	Description
Digital Pins			
FOUTL,R	30, 31	O	Filter outputs left, right. A.C. coupled externally to CIN L,R in order to remove DC offsets. These outputs have internal series resistors of about 5K ohms. Capacitors to analog ground on these pins can be used to create a lowpass filter pole that removes switching noise introduced by the switched-capacitor filters.
CINL,R	40, 41	I	Capacitive coupled inputs left, right. These inputs have internal pull-up resistors to CMR of approximately 50K ohms.
VREF	42	O	Reference generator resistor divider output. Should be bypassed to analog ground with 0.1 uf capacitor.
CMR	43	O	Buffered reference output. Should be bypassed to analog ground with a 47 uf electrolytic capacitor with a .1 uf capacitor in parallel.
AOUT L,R	46, 47	O	Line level stereo outputs, left, right.
REFSEL	38	I	Option input. Analog GND: normal operation Analog VDD: reserved.
PCSPKO	50	O	Analog output of PCSPKI with volume control.
FDXO	49	O	Normally connected to CMR via an internal resistor. Can be programmed to connect internal to FOUT R pin during DSP serial mode.
FDXI	48	I	Input with internal pull-up to CMR. Alternate input to left channel filter stage in DSP serial mode.

2.6 Philips 87C552 System Management Controller

The 87C552 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 87C552 has the same instruction set as the 80C51.

The 87C552 contains a 8kx8 a volatile 256x8 read/write data memory, five 8-bit I/O ports, one 8-bit input port, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a 15-source, two-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC pulse width modulated interface, two serial interfaces (UART and I^2C-bus), a “watchdog” timer and on-chip oscillator and timing circuits. For systems that require extra capability, the 87C552 can be expanded using standard TTL compatible memories and logic.

In addition, the 87C552 has two software selectable modes of power reduction—idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial ports, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte, and 17 three-byte. With a 16MHz (24MHz) crystal, 58% of the instructions are executed in 0.75ms (0.5ms) and 40% in 1.5ms (1ms). Multiply and divide instructions require 3ms (2ms).

2.6.1 Features

- 80C51 central processing unit
- 8kx8 EPROM expandable externally to 64k bytes
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- Two standard 16-bit timer/counters
- 256x8 RAM, expandable externally to 64k bytes
- Capable of producing eight synchronized, timed outputs
- A 10-bit ADC with eight multiplexed analog inputs
- Two 8-bit resolution, pulse width modulation outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- I^2C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART compatible with the standard 80C51
- On-chip watchdog timer
- Speed ranges: 16MHz

- Extended temperature ranges
- OTP package available

2.6.2 Block Diagram

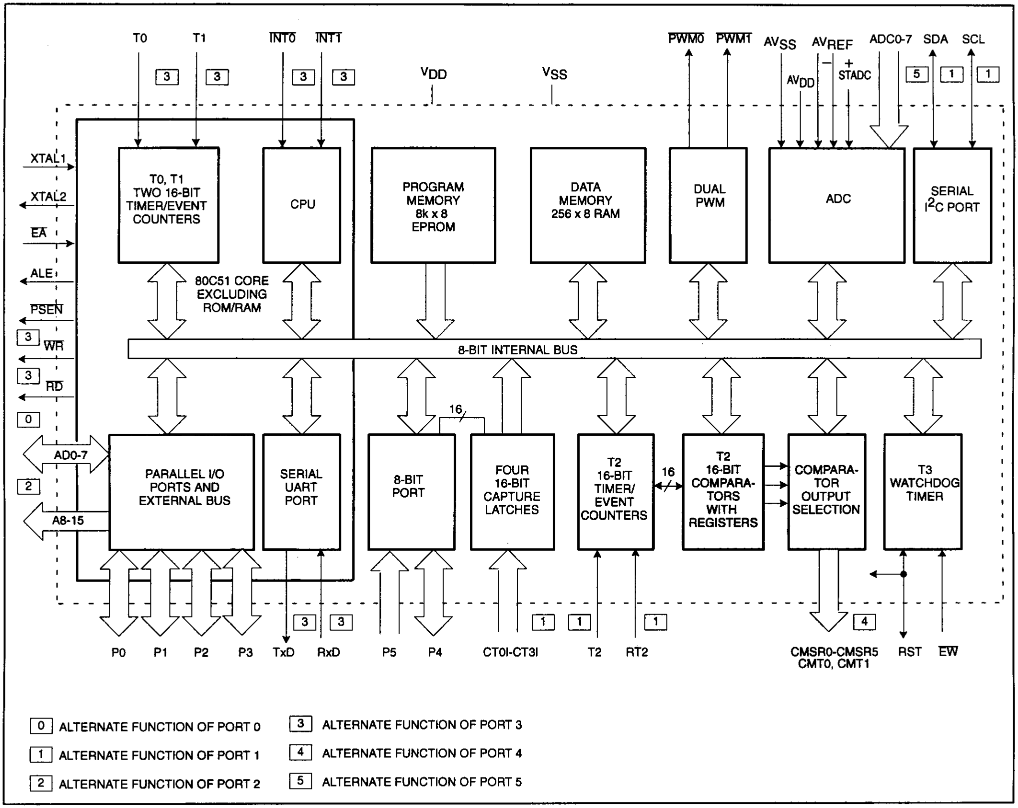


Figure 2-15 87C552 Block Diagram

2.6.3 Pin Diagram

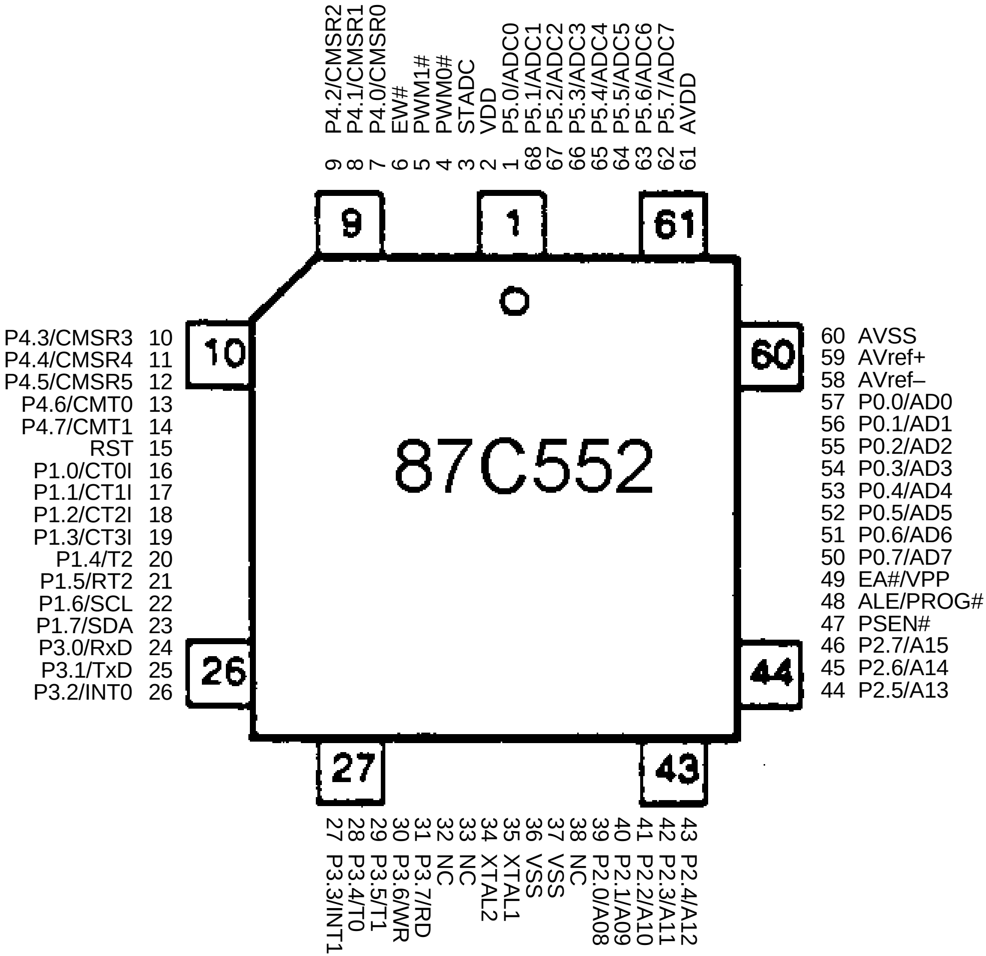


Figure 2-16 87C552 Pin Diagram

2.6.4 Pin Descriptions

Table 2-12 87C552 Pin Descriptions

Mnemonic	Pin No.	Type	Name And Function
V_{DD}	2	I	**Digital Power Supply:** +5V power supply pin during normal operation, idle and power-down mode.
STADC	3	I	**Start ADC Operation:** Input starting analog to digital conversion (ADC operation can also be started by software).
PWM0#	4	O	**Pulse Width Modulation:** Output 0.
PWM1#	5	O.	**Pulse Width Modulation:** Output 1
EW#	6	I	**Enable Watchdog Timer:** Enable for T3 watchdog timer and disable power-down mode.
P0.0-P0.7	57-50	I/O	**Port 0:** Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pull-ups when emitting 1s. Port 0 is also used to input the code byte during programming and to output the code byte during verification.
P1.0-P1.7	16-23	I/O	**Port 1:** 8-bit I/O port. Alternate functions include:
	16-21	I/O	**(P1.0-P1.5):** Quasi-bidirectional port pins.
	22-23	I/O	**(P1.6, P1.7):** Open drain port pins.
	16-19	I	**CT0I-CT3I (P1.0-P1.3):** Capture timer input signals for timer T2.
	20	I	**T2 (P1.4):** T2 event input.
	21	I	**RT2 (P1.5):** T2 timer reset signal. Rising edge triggered.
	22	I/O	**SCL (P1.6):** Serial port clock line I^2C-bus.
	23	I/O	**SDA (P1.7):** Serial port data line I^2C-bus. Port 1 is also used to input the lower order address byte during EPROM programming and verification. A0 is on P1.0, etc.
P2.0-P2.7	39-46	I/O	**Port 2:** 8-bit quasi-bidirectional I/O port. Alternate function: High-order address byte for external memory (A08-A15). Port 2 is also used to input the upper order address during EPROM programming and verification. A8 is on P2.0, A9 on P2.1, through A12 on P2.4.
P3.0-P3.7	24-31	I/O	**Port 3:** 8-bit quasi-bidirectional I/O port. Alternate functions include:
	24		**RxD(P3.0):** Serial input port.
	25		**TxD (P3.1):** Serial output port.
	26		**INT0 (P3.2):** External interrupt.
	27		**INT1 (P3.3):** External interrupt.
	28		**T0 (P3.4):** Timer 0 external input.
	29		**T1 (P3.5):** Timer 1 external input.
	30		**WR (P3.6):** External data memory write strobe.
	31		**RD (P3.7):** External data memory read strobe.

Table 2-12 87C552 Pin Descriptions (continued)

Mnemonic	Pin No.	Type	Name And Function
P4.0-P4.7	7-14	I/O	**Port 4:** 8-bit quasi-bidirectional I/O port. Alternate functions include:
	7-12	O	**CMSR0-CMSR5 (P4.0-P4.5):** Timer T2 compare and set/reset outputs on a match with timer T2. 13, 14
	13, 14	O	**CMT0, CMT1 (P4.6, P4.7):** Timer T2 compare and toggle outputs on a match with timer T2.
P5.0-P5.7	68-62,	I	**Port 5:** 8-bit input port.
	1		**ADC0-ADC7 (P5.0-P5.7):** Alternate function: Eight input channels to ADC.
RST	15	I/O	**Reset:** Input to reset the 87C552. It also provides a reset pulse as output when timer T3 overflows.
XTAL1	35	I	**Crystal Input 1:** Input to the inverting amplifier that forms the oscillator, and input to the internal clock generator. Receives the external clock signal when an external oscillator is used.
XTAL2	34	O	**Crystal Input 2:** Output of the inverting amplifier that forms the oscillator. Left open-circuit when an external clock is used.
V_{SS}	36, 37	I	**Digital ground.**
PSEN#	47	O	**Program Store Enable:** Active-low read strobe to external program memory.
ALE/PROG#	48	O	**Address Latch Enable:** Latches the low byte of the address during accesses to external memory. It is activated every six oscillator periods. During an external data memory access, one ALE pulse is skipped. ALE can drive up to eight LS TTL inputs and handles CMOS inputs without an external pull-up. This pin is also the program pulse input (PROG#) during EPROM programming.
EA#/V_{PP}	49	I	**External Access:** When EA# is held at TTL level high, the CPU executes out of the internal program ROM provided the program counter is less than 8192. When EA# is held at TTL low level, the CPU executes out of external program memory. EA# is not allowed to float. This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming.
AV_{REF-}	58	I	**Analog to Digital Conversion Reference Resistor:** Low-end.
AV_{REF+}	59	I	**Analog to Digital Conversion Reference Resistor:** High-end.
AV_{SS}	60	I	**Analog Ground**
AV_{DD}	61	I	**Analog Power Supply**

2.7 NS87336VLJ Super I/O Controller

The PC87336VLJ is a single chip solution for most commonly used I/O peripherals in ISA, and EISA based computers. It incorporates a Floppy Disk Controller(FDC), two full featured UARTs, and an IEEE 1284 compatible parallel port Standard PC-AT address decoding for all the peripherals and a set of configuration registers are also implemented in this highly integrated member of the Super I/O family. Advanced power management features, mixed voltage operation and integrated Serial-Infrared(both IrDA and Sharp) support makes the PC87336 an ideal choice for low-power and/or portable personal computer applications.

The PC87336 FDC uses a high performance digital data separator eliminating the need for any external filter components. It is fully compatible with the PC8477 and incorporates a superset of DP8473, NEC PD765 and N82077 floppy disk controller functions. All popular 5.25” and 3.5” floppy drives, including the 2.88 MB 3.5” floppy drive, are supported. In addition, automatic media sense and 2 Mbps tape drive support are provided by the FDC.

The two UARTs are fully NS16450 and NS16550 compatible. Both ports support MIDI baud rates and one port also supports IrDA’s the HP SIR and Sharp SIR compliant signaling protocol.

The parallel port is fully IEEE 1284 level 2 compatible. The SPP(Standard Parallel Port) is fully compatible wit ISA and EISA parallel ports. In addition to the SPP, EPP(Enhanced Parallel Port) and ECP(Extended Capabilities Port) modes are supported by the parallel port.

A set of configuration registers are provided to control the Plug and Play and other various functions of the PC87336. These registers are accessed using two 8-bit wide index and data registers. The ISA I/O address of the register pair can be relocated using a power-up strapping option and the software configuration after power-up.

When idle, advanced power management features allows the PC87336 to enter extremely low power modes under software control. The PC87336 can operate from a 5V or a 3.3V power supply. An unique I/O cell structure allows the PC87336 to interface directly with 5V external components while operating from a 3.3V power supply.

2.7.1 Features

- 100% compatible with ISA, and EISA architectures
- The Floppy Disk Controller:
  - Software compatible with the DP8473, the 765A and the N82077
  - 16-byte FIFO(disabled by default)
  - Burst and Non-Burst modes
  - Perpendicular Recording drive support
  - New high-performance internal digital data separator(no external filter components required)
  - Low-power CMOS with enhanced power-down mode
  - Automatic media-sense support, with full IBM TDR(Tape Drive Register) implementation
  - Supports fast 2 Mbps and standard 1 Mbps/500 kbps/250 kbps tape drives

- The Bidirectional Parallel Port:
  - Enhanced Parallel Port(EPP) compatible
  - Extended Capabilities Port(ECP) compatible, including level 2 support
  - Bidirectional under either software or hardware control
  - Compatible with ISA, and EISA, architectures
  - Ability to multiplex FDC signals on parallel port pins allows use of an external Floppy Disk Drive(FDD)
  - Includes protection circuit to prevent damage to the parallel port when a connected printer is powered up or is operated at a higher voltage
- The UARTs:
  - Software compatible with the PC16550A and PC16450
  - MIDI baud rate support
  - Infrared support on UART2(IrDA and Sharp-compliant)
- The Address Decoder
  - 6 bit or 10 bit decoding
  - External Chip Select capability when 10 bit decoding
  - Full relocation capability(No limitation)
- Enhanced Power Management
  - Special configuration registers for power-down
  - Enhanced programmable power-down FDC command
  - Auto power-down and wake-up modes
  - 2 special pins for power management
  - Typical current consumption during power-down is less than 10 uA
  - Reduced pin leakage current
- Mixed Voltage support
  - Supports standard 5V operation
  - Supports 3.3V operation
  - Supports mixed internal 3.3V operation with 3.3V/5V external configuration
- The General Purpose Pins:
  - 2 pins, for 2 separate programmable chip select decoders, can be programmed for game port control

- Plug and Play Compatible:
    - 16 bit addressing(full programmable)
    - 10 selectable IRQs
    - 3 selectable DMA Channels
    - 3 SIRQ Inputs allows external devices to mapping IRQs
- 100-Pin TQFP package - PC87336VLJ

2.7.2 Block Diagram

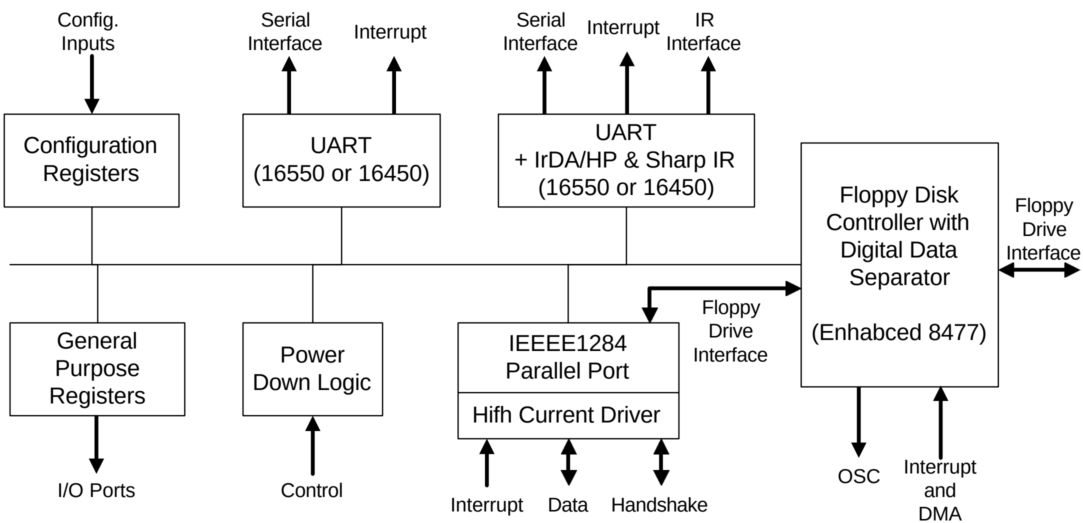


Figure 2-13 NS87336VLJ Block Diagram

2.7.3 Pin Diagram

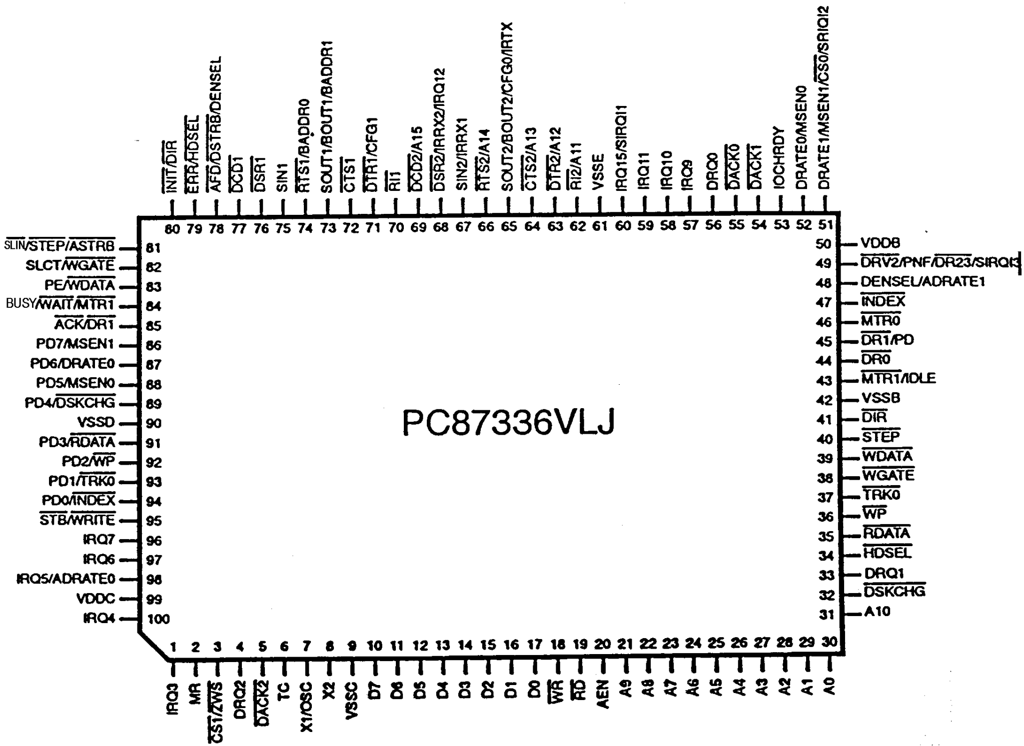


Figure 2-14 NS87336VLJ Pin Diagram

2.7.4 Pin Description

Table 2-10 NS87336VLJ Pin Descriptions

Pin	No.	I/O	Description
A15-A0	69, 66, 64:62, 31, 21:30	I	**Address.** These address lines from the microprocessor determine which internal register is accessed. A0-A15 are don't cares during DMA transfer.
/ACK	85	I	**Parallel Port Acknowledge.** This input is pulsed low by the printer to indicate that it has received the data from the parallel port. This pin has a nominal 25 KΩ pull-up resistor attached to it.
ADRATE0, ADRATE1	98, 48	O	**FDD Additional Data Rate 0,1.** These outputs are similar to DRATE0, 1. They are provided in addition to DRATE0, 1. They reflect the currently selected FDC data rate, (bits 0 and 1 in the Configuration Control Register (CCR) or the Data Rate Select Register (DSR), whichever was written to last). ADRATE0 is configured when bit 0 of ASC is 1. ADRATE1 is configured when bit 4 of ASC is 1. (See IRQ5 and DENSEL for further information).
/AFD	78	I/O	**Parallel Port Automatic Feed XT.** When this signal is low, the printer automatically line feed after printing each line. This pin is in a tristate condition 10 ns after a 0 is loaded into the corresponding Control Register bit. The system should pull this pin high using a 4.7 KΩ resistor.
AEN	20	I	**Address Enable.** When this input is high, it disables function selection via A15-A0. Access during DMA transfer is not affected by this pin.
/ASTRB	81	O	**EPP Address Strobe.** This signal is used in EPP mode as address strobe. It is an active low signal.
BADDR0, BADDR1	74, 73	I	**Base Address.** These bits determine one of the four base addresses from which the Index and Data Registers are offset. An internal pull-down resistor of 30 KΩ is on this pin. Use a 10 KΩ resistor to pull this pin to VCC.
BOUT1, BOUT2	73 65	O	**UARTs Baud Output.** This multi-function pin supports the associated serial channel Baud Rate generator output signal if the test mode is selected in the Power and Test Configuration Register and the DLAB bit (LCR7) is set. After the Master Reset, this pin offers the SOUT function.
BUSY	84	I	**Parallel Port Busy.** This pin is set high by the printer when it cannot accept another character. It has a nominal 25 KΩ pull-down resistor attached to it.
CFG0 CFG1	65 71	I	**Configuration on Power-up.** These CMOS inputs select 1 of 4 default configurations in which the PC87336 powers up. An internal pull-down resistor of 30 KΩ is on each pin. Use a 10 KΩ resistor to pull these pins to VCC.

Table 2-10 NS87336VLJ Pin Descriptions (continued)

Pin	No.	I/O	Description
/CS0, /CS1	51, 3	O	**Programmable Chip Select.** /CS0, 1 are programmable chip select and/or latch enable and/or output enable signals that can be used as game port, I/O expand, etc. The decoded address and the assertion conditions are configured via the 87336VLJ's configuration registers.
/CTS1, /CTS2	72, 64	I	**UARTs Clear to Send.** When low, this indicates that the modem or data set is ready to exchange data. The /CTS signal is a modem status input. The CPU tests the condition of this /CTS signal by reading bit 4 (CTS) of the Modem Status Register (MSR) for the appropriate serial channel. Bit 4 is the complement of the CTS signal. Bit 0 (DCTS) has no effect on the transmitter. /CTS2 is multiplexed with A13. When it is not selected, it is masked to "0". **NOTE:** *Whenever the MSR DCTS bit is set, an interrupt is generated if Modem Status interrupts are enabled.*
D7-D0	10-17	I/O	**Data.** These are bidirectional data lines to the microprocessor. D0 is the LSB and D7 is the MSB. These signals have a 24 mA (sink) buffered outputs.
/DACK0 /DACK1 /DACK2	5, 54 55	I	**DMA Acknowledge 0, 1, 2.** These active low inputs acknowledge the DMA request and enable the /RD and /WR inputs during a DMA transfer. It can be used by one of the following: FDC or Parallel Port. If none of them uses this input pin, it is ignored. If the device which uses on of this pins is disabled or configured with no DMA, this pin is also ignored. /DACK0, 1, 2should be held high during I/O accesses.
/DCD1, /DCD2	77 69	I	**UARTs Data Carrier Detect.** When low, this indicates that the modem or data set has detected the data carrier. The /DCD signal is a modem status input. The CPU tests the condition of this /DCD signal by reading bit 7 (DCD) of the Modem Status Register (MSR) for the appropriate serial channel. Bit 7 is the complement of the DCD signal. Bit 3 (DDCD) of the MSR indicates whether DCD input has changed state since the previous reading of the MSR. **NOTE:** *Whenever the MSR DDCD bit is set, an interrupt is generated if Modem Status interrupts are enabled.*

Table 2-10 NS87336VLJ Pin Descriptions (continued)

Pin	No.	I/O	Description
DENSEL (Normal Mode)	48	O	**FDC Density Select.** DENSEL indicates that a high FDC density data rate (500 Kbs, 1 Mbs or 2 Mbs) or a low density data rate (250 or 300 Kbs) is selected. DENSEL is active high for high density (5.25-inch drives) when IDENT is high, and active low for high density (3.5-inch drives) when IDENT is low. DENSEL is also programmable via the Mode command.
DENSEL (PPM Mode)	78	O	**FDC Density Select.** This pin offers an additional Density Select signal in PPM Mode when PNF=0.
/DIR (Normal Mode)	41	O	**FDC Direction.** This output determines the direction of the floppy disk drive (FDD) head movement (active = step-in; inactive = step-out) during a seek operation. During reads or writes, DIR is inactive.
/DIR (PPM Mode)	80	O	**FDC Direction.** This pin offers an additional Direction signal in PPM Mode when PNF = 0.
/DR0, /DR1 (Normal Mode)	44, 45	O	**FDC Drive Select 0, 1.** These are the decoded drive select outputs that are controlled by Digital Output Register bits D0, D1. The Drive Select outputs are gated with DOR bits 4-7. These are active low outputs. They are encoded with information to control four FDDs when bit 4 of the Function Enable Register (FER) is set. DR0 exchanges logical drive values with DR1 when bit 4 of Function Control Register is set.
/DR1 (PPM Mode)	85	O	**FDC Drive Select 1.** This pin offers an additional Drive Select signal in PPM Mode when PNF = 0. It is drive select 1 when bit 4 of FCR is 0. It is drive select 0 when bit 4 of FCR is 1. This signal is active low.
/DR23	49	O	**FDC Drive 2 or 3.** /DR23 is asserted when either Drive 2 or Drive 3 is assessed(except during logical drive exchange).
/DRATE0 /DRATE1 (Normal Mode)	52, 51	O	**FDC Data Rate 0, 1.** These outputs reflect the currently selected FDC data rate (bits 0 and 1 in the Configuration Control Register (CCR) or the Data Rate Select Register (DSR), whichever was written to last). The pins are totem-pole buffered outputs (6 mA sink, 6 mA source).
/DRATE0 (PPM Mode)	87	O	**FDC Data Rate 0.** This pin provides an additional Data Rate signal, in PPM mode, When PNF=0.
DRQ0 DRQ1 DRQ2	56 33 4	O	**DMA Request 0, 1, 2.** \An active high output that signals the DMA controller that a data transfer is required. This DMA request can be sourced by one of the following: FDC or Parallel Port. When it is not sourced by and of them, it is in TRI-STATE. When the sourced device is disabled or when the sourced device is configured with no DMA, it is also in TRI-STATE. Upon reset, DRQ2 is used by the FDC.

Table 2-10 NS87336VLJ Pin Descriptions (continued)

Pin	No.	I/O	Description
/DRV2	49	I	**FDD Drive2.** This input indicates whether a second disk drive has been installed. The state of this pin is available from Status Register A in PS/2 mode. (See PNF for further information).
/DSKCHG (Normal Mode)	32	I	**Disk Change.** The input indicates if the drive door has been opened. The state of this pin is available from the Digital Input Register. This pin can also be configured as the RGATE data separator diagnostic input via the Mode command.
/DSKCHG (PPM Mode)	89	I	**Disk Change.** This pin offers an additional Disk Change signal in PPM Mode when PNF = 0.
/DSR1 /DSR2	76, 68	I	**UARTs Data Set Ready.** When low, this indicates that the data set or modem is ready to establish a communications link. The DSR signal is a modem status input. The CPU tests the /DSR signal by reading bit 5 (DSR) of the Modem Status Register (MSR) for the appropriate channel. Bit 5 is the complement of the DSR signal. Bit 1 (DDSR) of the MSR indicates whether the DSR input has changed state since the previous reading of the MSR. **NOTE:** *Whenever the DDSR bit of the NSR is set, an interrupt is generated if Modem Status interrupts are enabled.*
/DSTRB	78	O	**EPP Data Strobe.** This signal is used in EPP mode as data strobe. It is an active low signal.
/DTR1 /DTR2	71, 63	O	**UARTs Data Terminal Ready.** When low, this output indicates to the modem or data set that the UART is ready to establish a communications link. The DTR signal can be set to an active low by programming bit 0 (DTR) of the Modem Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal to its inactive state.
/ERR	79	I	**Parallel Port Error.** This input is set low by the printer when an error is detected. This pin has a nominal 25 KOHM pull-up resistor attached to it.
/HDSEL (Normal Mode)	34	O	**FDC Head Select.** This output determines which side of the FDD is accessed. Active selects side 1, inactive selects side 0.
/HDSEL (PPM Mode)	79	O	**FDC Head Select.** This pin offers an additional Head Select signal in PPM Mode when PNF = 0.
IDLE	43	O	**FDD IDLE.** IDLE indicates that the FDC is in the IDLE state and can be powered down. Whenever the FDC is in IDLE state, or in power-down state, the pin is active high.
/INDEX	47	I	**Index.** This input signals the beginning of a FDD track.
/INDEX (Normal Mode)	94	I	**Index.** This pin gives an additional Index signal in PPM mode when PNF = 0.
/INIT (PPM Mode)	80	I/O	**Initialize.** When this signal is low, it causes the printer to be initialized. This pin is in a tristate condition 10 ns after a 1 is loaded into the corresponding Control Register bit. The system should pull this pin high using a 4.7 KΩ resistor.

Table 2-10 NS87336VLJ Pin Descriptions (continued)

Pin	No.	I/O	Description
IORCHDY	53	O	**I/O Channel Ready.** When IORCHDY is driven low, the EPP extends the host cycle.
IRQ3, 4 IRQ5-7 IRQ9-11 IRQ12, 15	1, 100 98-96, 57-59, 68, 60	I/O	**Interrupt 3, 4, 5, 6, 7, 9, 10, 11, 12, and 15.** This pin can be a totem-pole output or an open-drain output. The interrupt can be sourced by one of the following: UART1 and/or UART2, parallel port, FDC, SIRQI1 pin, SIRQI2 pin or SIRQI3 pin. IRQ5 is multiplexed with ADRATE0. IRQ12 is multiplexed with /DSR2 and IRRX2. IRQ15 is multiplexed with SIRQ11.
IRRX1 IRRX2	67, 68	I	**IrDA or SHARP- Infrared Receive.** One of these pins is the infrared serial data input. IRRX1 is multiplexed with SIN2. IRRX2 is multiplexed with /DSR2 and IRQ12.
IRTX	65	O	**Infrared Transmit. I**nfrared serial data output. Software configuration selects either IrDA or Sharp-IR protocol. This pin is multiplexed with SOUT2/BOUT/CFG0.
MR	2	I	**Master Reset.** Active high output that resets the controller to the idle state and resets all disk interface outputs to their inactive states. The DOR, DSR, CCR, Mode command, Configure command, and Lock command parameters are cleared to their default values. The Specify command parameters are not affected

Table 2-10 NS87336VLJ Pin Descriptions (continued)

Pin	No.	I/O	Description
/MSEN0 /MSEN1 (Normal Mode)	52, 51	I	**Media Sense.** These pins are Media Sense input pins when bit 0 of FCR is 0. Each pin has a 10 KΩ internal pull-up resistor. When bit 0 of FCR is 1, these pins are Data Rate output pins and the pull-up resistors are disabled.
/MSEN0 /MSEN1 (PPM Mode)	88, 86	I	**Media Sense.** These pins gives additional Media Sense signals for PPM Mode and PNF = 0.
/MTR0 /MTR1 (Normal Mode)	46, 43	O	**FDC Motor Select 0, 1.** These are the motor enable lines for drives 0 and 1, and are controlled by bits D7-D4 of the Digital Output register. They are active low outputs. They are encoded with information to control four FDDs when bit 4 of the Function Enable Register (FER) is set. MTR0 exchanges logical motor values with MTR1 when bit 4 of FCR is set.
/MTR1 (PMM Mode)	84	O	**FDC Motor Select 1.** This pin offers an additional Motor Select 1 signal in PPM mode when PNF = 0. This pin is the motor enable line for drive 1 when bit 4 of FCR is 0. It is the motor enable line for drive 0 when bit 4 of FCR 1. This signal is active low
PD	45	O	**FDC Power Down.** This pin is PD output when bit 4 of PMC is 1. It is /DR1 when bit 4 of PMC is 0. PD is active high whenever the FDC is in power-down state, either via bit 6 of the DSR (or bit 3 of FER, or bit 0 of PTR), or via the mode command.
PD0-7	94-91, 89-86	I/O	**Parallel Port Data.** These bidirectional pins transfer data to and from the peripheral data bus and the parallel port Data Register. These pins have high current drive capability.
PE	83	I	**Parallel Port Paper End.** This input is set high by the printer when it is out of paper. This pin has a nominal 25 KΩ pull-down resistor attached to it.
PNF	49	I	**Printer Not Floppy.** PNF is the Printer Not Floppy pin when bit 2 of FCR is 1. It selects the device which is connected to the PPM pins. A parallel printer is connected when PNF = 1 and a floppy disk drive is connected when PNF = 0. This pin is the DRV2 input pin when bit 2 of FCR is 0.
/RD	19	I	**Read.** Active low input to signal a data read by the microprocessor.
/RDATA (Normal Mode)	35	I	**FDD Read Data.** This input is the raw serial data read from the floppy disk drive.
/RDATA (PPM Mode)	91	I	**FDD Read Data.** This pin supports an additional Read Data signal in PPM Mode when PNF = 0.

Table 2-10 NS87336VLJ Pin Descriptions (continued)

Pin	No.	I/O	Description
/RI1 /RI2	70, 62	I	**UARTs Ring Indicator.** When low, this indicates that a telephone ring signal has been received by the modem. The /RI signal is a modem status input whose condition is tested by the CPU by reading bit 6 (RI) of the Modem Status Register (MSR) for the appropriate serial channel. Bit 6 is the complement of the RI signal. Bit 2 (TERI) of the MSR indicates whether the RI input has changed from low to high since the previous reading of the MSR. **NOTE:** *When the TERI bit of the MSR is set and Modem Status interrupts are enabled, an interrupt is generated.*
/RTS1 /RTS2	74, 66	O	**UARTs Request to Send.** When low, this output indicates to the modem or data set that the UART is ready to exchange data. The RTS signal can be set to an active low by programming bit 1 (RTS) of the Modem Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal to its inactive state.
SIN1 SIN2	75, 67	I	**UARTs Serial Input.** This input receives composite serial data from the communications link (peripheral device, modem, or data set).
SIRQ1 SIRQ2 SIRQ4	60, 51, 49	I	**System interrupt 1, 2, and 3.** This input can be routed to one of the following output pins: IRQ3-IRQ7, IRQ9-IRQ12. SIRQ12 and SIRQ13 can be also routed to IRQ15. Software configuration determines to which output pin the input pin is routed to. SIRQ1 is multiplexed with IRQ15, SRIQ12 is multiplexed with DRATE1/MSEN1/CS0, and SIRQ3 is multiplexed with DRV2/PNF/DR23.
SLCT	82	I	**Parallel Port Select.** This input is set high by the printer when it is selected. This pin has a nominal 25 KΩ pull-down resistor attached to it.
/SLIN	81	I/O	**Parallel Port Select Input.** When this signal is low, it selects the printer. This pin is in a tristate condition 10 ns after a 0 is loaded into the corresponding Control Register bit. The system should pull this pin high using a 4.7 KΩ resistor.
SOUT1 SOUT2	73, 65	O	**UARTs Serial Output.** This output sends composite serial data to the communications link (peripheral device, modem, or data set). The SOUT signal is set to a marking state (logic 1) after a Master Reset operation.
/STB	95	I/O	**Parallel Port Data Strobe.** This output indicates to the printer that a valid data is available at the printer port. This pin is in a tristate condition 10 ns after a 0 is loaded into the corresponding Control Register bit. The system should pull high using a 4.7 KΩ.
/STEP (Normal Mode)	40	O	**FDC Step.** This output signal issues pulses to the disk drive at a software programmable rate to move the head during a seek operation.
/STEP (PPM Mode)	81	O	**FDC Step.** This pin gives an additional step signal in PPM Mode when PNF = 0.

Table 2-10 NS87336VLJ Pin Descriptions (continued)

Pin	No.	I/O	Description
TC	6	I	**Terminal Count.** Control signal from the DMA controller to indicate the termination of a DMA transfer. TC is accepted only when FDACK is active. TC is active high in PC-AT and Model 30 modes, and active low in PS/2 mode.
/TRK0 (Normal Mode)	37	I	**FDC Track 0.** This input indicates the controller that the head of the selected floppy disk drive is at track zero.
/TRK0 (PPM Mode)	93	I	**FDC Track 0.** This pin gives an additional Track 0 signal in PPM Mode when PNF = 0.
VDDB, C	50, 99		**Power Supply.** This is the 3.3V/5V supply voltage for the 87336VLJ circuitry.
VSSB-E	42, 9, 90, 61		**Ground.** This is the ground for the 87336VLJ circuitry.
/WAIT	84	I	**EPP Wait.** This signal is used in EPP mode by the parallel port device to extend its access cycle. It is an active low signal.
/WDATA (Normal Mode)	39	O	**FDC Write Data.** This output is the write precompensated serial data that is written to the selected floppy disk drive. Precompensation is software selectable.
/WDATA (PPM Mode)	83	O	**FDC Write Data.** This pin provides an additional Write Data signal in PPM Mode when PNF=0. (See PE.)
/WGATE (Normal Mode)	38	O	**FDC Write Gate.** This output signal enables the write circuitry of the selected disk drive. WGATE has been designated to prevent glitches during power-up and power-down. This prevents writing to the disk when power is cycled.
/WGATE (PPM Mode)	82	O	**FDC Write Gate.** This pin gives an additional Write Gate signal in PPM mode when PNF = 0.
/WP (Normal Mode)	36	I	**FDC Write Protect.** This input indicates that the disk in the selected drive is write protected.
/WP (PPM Mode)	92	I	**FDC Write Protect.** This pin gives an additional Write Gate signal in PPM mode when PNF = 0.
/WR	18	I	**Write.** An active low input to signal a write from the microprocessor to the controller.
/WRITE	95	O	**EPP Write Strobe.** This signal is used in EPP mode as write strobe. It is active low.
X1/OSC	7	I	**Crystal1/Clock.** One side of an external 24 MHz/48 MHz crystal is attached here. If a crystal is not used, a TTL or CMOS compatible clock is connected to this pin.
X2	8	O	**Crystal 2.** One side of an external 24 MHz/48 MHz crystal is attached here. This pin is left unconnected if an external clock is used.
/ZWS	3	O	**Zero Wait State.** This pin is the Zero Wait State open drain output pin when bit 6 of FCR is 0. ZWS is driven low when the EPP or ECP is written, and the access can be shortened.

2.8 CL-PD6730 PCI PCMCIA Controller

The CL-PD6730 is a single-chip PC Card host adapter solution capable of controlling two fully independent PC Card sockets. The chip is compliant with PC Card Standard, PCMCIA 2.1, and JEIDA 4.1 and is optimized for use in notebook and handheld computers where reduced form factor and low power consumption are critical design objectives.

The CL-PD6730 chip employs energy-efficient, mixed-voltage technology that can reduce system power consumption by over 50 percent. The chip also provides a Suspend mode and an automatic Low-Power Dynamic mode, which stop transactions on the PC Card bus, stop internal clock distribution, and turn off much of the internal circuitry.

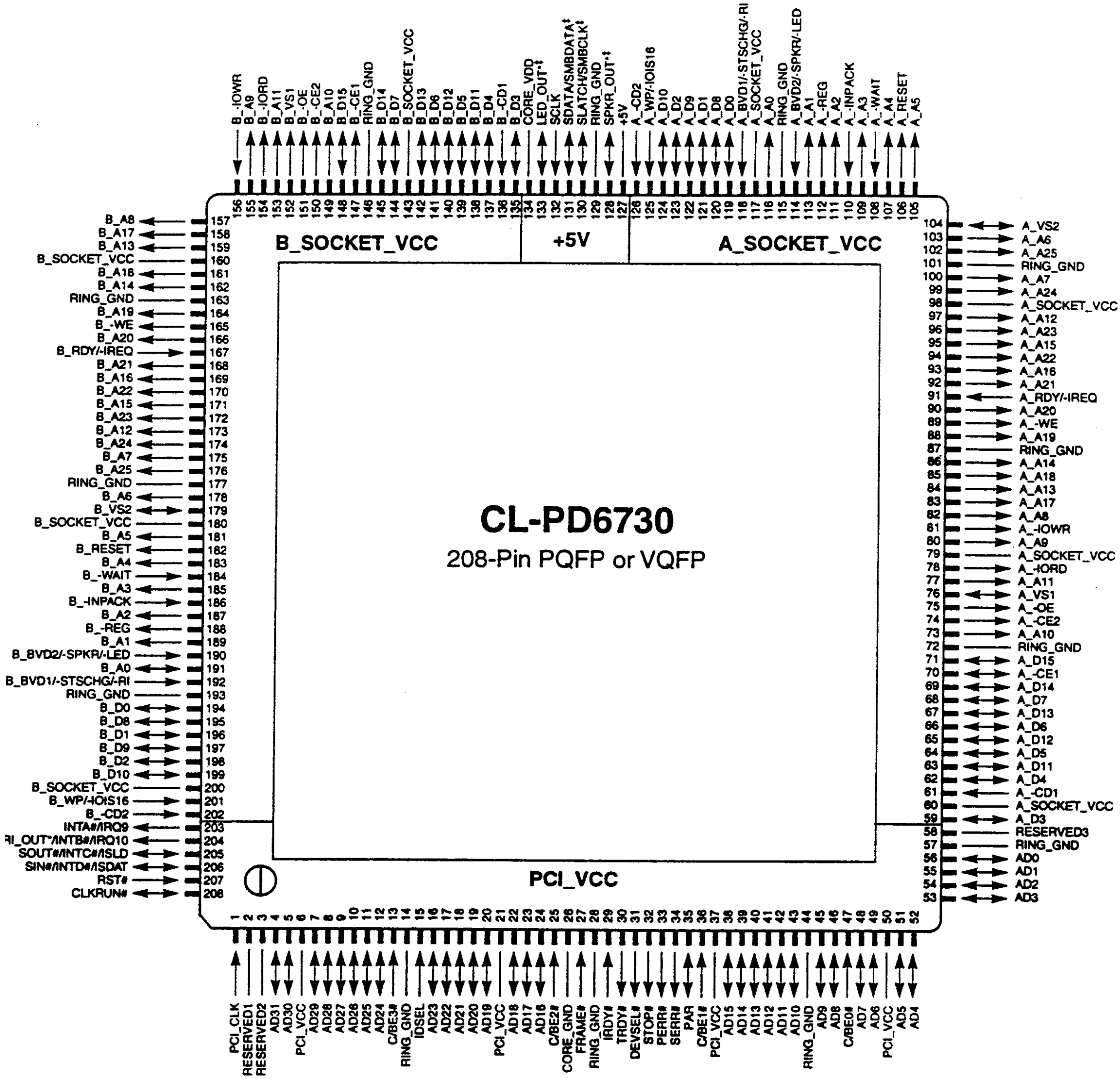
PC applications typically access PC Cards through the socket/card-services software interface. To assure full compatibility with existing socket/card-services software and PC Card applications, the register set in the CL-PD6730 is a superset of the CL-PD6729 register set.

The chip provides fully buffered PC Card interfaces, meaning that no external logic is required for buffering signals to/from the interface, and power consumption can be controlled by limiting signal transitions on the PC Card bus.

2.8.1 Features

- Single-chip PC Card host adapter
- Direct connection to PCI bus and two PC Card sockets
- Compliant with PCI 2.1, PC Card Standard, and JEIDA 4.1
- CL-PD672X-compatible register set, ExCA™-compatible
- Programmable interrupt protocol: PCI, PC/PCI, External-Hardware, or PCUUtay interrupt signaling modes
- Serial interface to power control devices
- Automatic Low-Power Dynamic mode for lowest power consumption
- Programmable Suspend mode
- Five programmable memory windows per socket
- Two programmable I/O windows per socket
- ATA disk interface support
- Mixed-voltage operation (3.3/5.0 V)
- Supports low-voltage PC Card specification
- 200 pin PQFP

2.8.2 Pin Diagram



2.8.3 Pin Descriptions

Pin signal type annotation

The following conventions apply to the pin signals.

- A pound sign (#) at the end of a pin name indicates an active-low signal for the PCI bus.
- A dash (-) at the beginning of a pin name indicates an active-low signal for the PC Card bus.
- An asterisk (*) at the end of a pin name indicates an active-low signal that is a general-interface for the CL-PD6730.

- A double-dagger superscript (‡) at the end of the pin name indicates signals that are used for power-on configuration switches.

- The I/O-type code (I/O) column indicates the input and output configurations of the pins on the CL-PD6730.The possible types are defined below. The possible types are defined below.

I/O Type	Description
I	Input pin
I-PU	Input pin with internal pull-up resistor
O	Constant-driven output pin
I/O	Input/output pin
O-OD	Open-drain output pin
O-TS	Tristate output pin
GND	Ground pin
PWR	Power pin

- The power-type code (Pwr.) column indicates the output drive power source for an output pin or the pull-up power source for an input pin on the CL-PD6730. The possible types are defined below.

Power Type	Output or Pull-up Power Source
1	+5v: powered from a 5-volt power supply (in most systems, see description of +5V pin in Table 2-4)
2	A_SOCKET_VCC: powered from the Socket A Vcc supply connecting to PC Card pins 17 and 51 of Socket A
3	B_SOCKET_VCC: powered from the Socket B Vcc supply connecting to PC Card pins 17 and 51 of Socket B
4	PCI_VCC: powered from the PCI bus power supply
5	CORE_VDD: powered from a 3.3-volt power supply

The following table lists the pin descriptions

Table 2-14 CL-PD6730 Pin Descriptions

Pin Name	Description	Pin Number	I/O	Power
PCI Bus Interface Pins				
AD[31:0]	**PCI Bus Address Input / Data Input/Output:** These pins connect to PCI bus signals AD[31:0].	4, 5, 7-12, 16-20, 22-24, 48 49, 51-56	I/O	4
C/BE[3:0]#	**PCI Bus Command / Byte Enable:** The command signaling and byte enables are multiplexed on the same pins. During the address phase of a transaction, C/BE[3:0]# are interpreted as the bus commands. During the data phase, C/BE[3:0]# are interpreted as byte enables. The byte enables are to be valid for the entirety of each data phase, and they indicate which bytes in the 32-bit data path are to carry meaningful data for the current data phase.	13, 25, 36, 47		
FRAME#	**Cycle Frame:** This input indicates to the CL-PD6730 that a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in its final phase.	27	I	
IRDY#	**Initiator Ready:** This input indicates the initiating agent's ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#.	29	I	
TRDY#	**Target Ready:** This output indicates the CL-PD6730's ability to complete the current data	30	O-TS	4
STOP#	**Stop:** This output indicates the current target is requesting the master to stop the current transaction.	32	O-TS	4
IDSEL	**Initialization Device Select:** This input is used as a chip select during configuration read and write transactions. This is a point-to-point signal. The CL-PD6730 must be connected to its own unique IDSEL line (from the PCI bus arbiter or one of the high-order AD bus pins).	15		
DEVSEL#	**Device Select:** The CL-PD6730 drives this output active (low) when it has decoded the PCI dress PC as one that it is programmed to support, thereby acting as the target for the current PCI cycle.	31	O-TS	4

Table 2-14 CL-PD6730 Pin Descriptions (continued)

Pin Name	Description	Pin Number	I/O	Power
PCI Bus Interface Pins (continued)				
PERR#	**Parity Error:** The CL-PD6730 drives this input active (low) if it detects a data parity error during a write phase.	33	O-TS	4
SERR#	**System Error:** This output is pulsed by the CL-PD6730 to indicate an address parity error.	34	O-TS	4
PAR	**Parity:** This pin is sampled the clock cycle after completion of each corresponding address or write data phase. For read operations this pin is driven from the cycle after TRDY# is asserted until the cycle after completion of each data phase. It ensures even parity across AD[31:0] and C/BE[3:0]#.	35	I/O	4
PCI_CLK	**PCI Clock:** This input provides timing for all transactions on the PCI bus to and from the CL-PD6730. All PCI bus interface signals described in this table, except RST#, INTA#, INTB#, INTC#, and INTD#, are sampled and driven on the rising edge of PCI_CLK; and all CL-PD6730 PCI bus interface timing parameters are defined with respect to this edge. This input can be operated at frequencies from 0 to 33 MHz. Note that the PC Card socket interface cannot operate at more than 25 MHz.	1		
RST#	**Device Reset:** This input is used to initialize all registers and internal logic to their reset states and place most CL-PD6730 pins in a high-impedance state.	207		
INTA#/ IRQ9	**PCI Bus Interrupt A / ISA Interrupt Request 9:** This output indicates a programmable interrupt request generated from any of a number of card actions. Although there is no specific mapping requirement for connecting interrupt lines from the CL-PD6730 to the system, a common use is to connect this pin to the PCI bus INTA# interrupt line and using PCI Interrupt Signaling mode. In External-Hardware Interrupt Signaling mode, this pin indicates interrupt request IRQ9.	203	O-TS	4

Table 2-14 CL-PD6730 Pin Descriptions (continued)

Pin Name	Description	Pin Number	I/O	Power
PCI Bus Interface Pins (continued)				
RI_OUT*/ INTB#/ IRQ10	**Ring Indicate Output / PCI Bus Interrupt B / ISA Interrupt Request 10:** In PCI Interrupt Signaling mode, this output can be used as an interrupt output connected to the PCI bus INTB# interrupt line. In External-Hardware Interrupt Signaling mode, this pin indicates interrupt request IRQ10.	204	O-TS	4
SOUT#/ INTC#/ ISLD	**Serial Interrupt Output / PCI Bus Interrupt C / Serial IRQ Load:** In PCI Interrupt Signaling mode, this output can be used as an interrupt output connected to the PCI bus INTC# interrupt line. In PC/PCI Serial Interrupt Signaling mode, this pin is the serial interrupt output, SOUT#. In External-Hardware Interrupt Signaling mode, this pin is the load signal, ISLD, used to load the serially transmitted interrupt data into the external serial-to-parallel shifters.	205	I/O	4
SIN# /INTD# /ISDAT	**Serial Interrupt Input / PCI Bus Interrupt D / Serial IRQ Data:** In PCI Interrupt Signaling mode, his output can be used as an interrupt output connected to the PCI bus INTD# interrupt line. In PC/PCI Serial Interrupt Signaling mode, this pin is the serial interrupt input, SIN#. In External-Hardware Interrupt Signaling mode, this pin is the IRQ vector data, ISDAT, that is serially transmitted to the external serial-to-parallel shifters.	206	I/O	4
CLKRUN#	**Clock Run:** This pin is an input to indicate the status of PCI_CLK or an open-drain output to request the starting or speeding up of PCI_CLK. This pin complies with the Mobile PCI Specification.	208	I/O	4
PCI_VCC	**PCI Bus Vcc:** These pins can be connected to either a 3.3- or 5-volt power supply. The PCI bus interface pin outputs listed in this table will operate at the voltage applied to these pins, independent of the voltage applied to other CL-PD6730 pin groups.	6, 21, 37, 50	PWR	

Table 2-14 CL-PD6730 Pin Descriptions (continued)

Pin Name	Description	Pin Number (socket A)	Pin Number (socket B)	I/O	Power
Socket Interface Pins					
REG	**Register Access:** In Memory Card Inter face mode, this output chooses between attribute and common memory. In I/O Card Interface mode, this signal is active (low). In ATA mode this signal is always high.	112	188\	O-TS	2 or 3
A[25:0]	**PC Card socket address outputs.**	102, 99, 98, 94, 92, 90, 88, 85, 83, 93, 95, 86, 84, 97, 77, 73, 80, 82, 175, 178, 105, 107, 109, 111, 113, 116	176, 174, 172, 170, 168,166, 164, 161, 158, 169, 171, 162, 159, 173, 153, 149, 155,157, 100, 103, 181, 183, 185, 187, 189, 191	O-TS	2 or 3
D[15:0]	**PC Card socket data I/O pins.**	71, 69, 67, 65,63, 124,68, 66,64, 62,59, 123,121, 119	148, 145,142, 140,138, 199,144 1415139, 137,135, 198,196, 194	I/O	2 or 3
-OE	**Output Enable:** This output goes active(low) to indicate a memory read from the PC Card socket to the CL-PD6730.	75	151	O-TS	2 or 3
-WE	**Write Enable:** This output goes active(low) to indicate a memory write from the CL-PD6730 to the PC Card socket.	89	165	O-TS	2 or 3
-IORD	**I/O Read:** This output goes active (low) for I/O reads from the socket to the CL-PD6730.	78	154	O-TS	2or3
-IOWR	**UO Write:** This output goes active (low) for I/O writes from the CL-PD6730 to the socket.	81	156	O-TS	2 or 3
WP/ -IOIS16	**Write Protect / UO** Is 16-Bit In Memory Card Interface mode, this input is interpreted as the status of the write protect switch on the PC Card. In I/O Card Interface mode, this input indicates the size of the I/O data at the current address on the PC Card.	125	201		

Table 2-14 CL-PD6730 Pin Descriptions (continued)

Pin Name	Description	Pin Number (socket A)	Pin Number (socket B)	I/O	Power
Socket Interface Pins (continued)					
-INPACK	**Input Acknowledge:** The -INPACK function is not applicable in PCI bus environments. However, for compatibility with other Cirrus Logic products, this pin should be connected to the PC Card socket's -INPACK pin.	110	1861	I-PU	2 or 3
RDY/ -IREQ	**Ready / Interrupt Request:** In Memory Card Interface mode, this input indicates to the CL-PD6730 that the card is either ready or busy. In I/O Card Interface mode, this input indicates a card interrupt request.	91	167	I-PU	2 or 3
-WAIT	**Wait:** This input indicates a request by the card to the CL-PD6730 to delay the cycle in progress until this signal is deasserted.	108	184	I-PU	2 or 3
-CD[2:1]	**Card Detect:** These inputs indicate to the CL-PD6730 that a card is in the socket. They are internally pulled high to the voltage of the +5V power pin.	126, 61	202, 136		I-PU
-CE[2:1]	**Card Enable:** These outputs are driven low by the CL-PD6730 during card access cycles to control byte/word card access. -CE1 enables even-numbered address bytes, and -CE2 enables odd-2 or 3 numbered address bytes. When configured for 8-bit cards, only -CE1 is active and A0 is used to indicate access of odd- or even-numbered bytes.	74, 70	150, 147		O*TS
RESET	**Card Reset:** This output is low for normal operation and goes high to reset the card. To prevent reset glitches to a card, this signal is high-impedance unless a card is seated in the socket, card power is applied, and the card's interface signals are enabled.	106	182	O-TS	2 or 3

Table 2-14 CL-PD6730 Pin Descriptions (continued)

Pin Name	Description	Pin Number (socket A)	Pin Number (socket B)	I/O	Power
Socket Interface Pins (continued)					
BVD2/ -SPKR/ -LED	**Battery Voltage Detect 2 / Speaker / LED:** In Memory Card Interface mode, this input serves as the BVD2 (battery warning status) input. In I/O Card Interface mode, this input can be configured to accept a card's -SPKR digital audio output. For ATA or non-ATA (SFF-68) disk-drive support, this input can also be configured as a drive-status LED input.	114	190	I-PU	2 or 3
BVD1/ -STSCHG/ -RI	**CBattery Voltage Detect 1 / Status change / Ring Indicate:** In Memory Card Interface mode, this input serves as the BVD1 (battery-dead status) input. in I/O Card Interface mode, this input is the -STSCHG input, which indicates to the CL-PD6730 that the card's internal status has changed.	118	192	I-PU	2 or 3
VS2	**Voltage Sense 2:** This pin is used in conjunction with VS1 to determine the operating voltage of the card. This pin is internally pulled high to the voltage of the +5V power pin. This pin connects to PC Card socket pin 57.	104	179	I/O-PU	1
VS1	**Voltage Sense 1:** This pin is used in conjunction with VS2 to determine the operating voltage of the card. This pin is internally pulled high to the voltage of the +5V power pin. This pin connects to PC Card socket pin 43.	76	152	I/O-PU	1
SOCKET _VCC	**Socket Vcc:** Connect these pins to the Vcc supply of the socket (pins 17 and 51 of the respective PC Card socket). These pins can be 0, 3.3, or 5 V, depending on card presence, card type, and system configuration. The socket interface out puts (listed in this table, Table 2-2) will operate at the voltage applied to these pins, independent of the voltage applied to other CL-PD6730 pin groups.	117, 98, 79, 60	200,180, 160, 143	PWR	

Table 2-14 CL-PD6730 Pin Descriptions (continued)

Pin Name	Description	Pin Number	I/O	Power
Power Control and General Interface Pins				
SPKR_OUT't	**Speaker Output:** This output can be used as a digital output to a speaker to allow a system to support PC Card fax/modem/voice and audio sound output. (for the socket whose speaker signal is to be directed from BVD2/-SPKR/-LED to this pin). This pin is used for configuration information during hardware reset.	128	I/O-PU	4
LED_OUT*t	**LED Output:** This output can be used as an LED driver to indicate disk activity when a socket's BVD2/-SPKR/-LED pin has been programmed for LED support. BVD2/-SPKR/-LED pin to reflect disk activity. This pin is used for configuration information during hardware reset.	133	I/O-PU	4
\SCLK	**Serial Clock:** This input is used as a reference clock (10-100 kHz, usually 32 kHz) to control the serial interface of the socket power control chips. CAUTION: This pin must be driven at all times.	132		
SDATA/ SMBDATA	**Serial Data / System Management Bus Data:** This pin serves as output pin SDATA when used with the serial interface of Texas Instruments' TPS22021DF socket power control chip, and serves as a bidirectional pin SMBDATA when used with Intel's System Management Bus used by Maxim's socket power control chip. This pin is used for configuration information during hardware reset.	131	I/O-PU	2 or 3
SLATCH/ SMBCLKt	**Serial Latch / System Management Bus Clock:** This pin serves as output pin SLATCH when used with the serial interface of Texas Instruments' TPS22021DF socket power control chip, and serves as a bidirectional pin SMBCLK hen used with Intel's System Management Bus used by Maxim's socket power control chip. This pin is used for configuration information during hardware reset.	130	I/O-PU	2 or3

Table 2-14 CL-PD6730 Pin Descriptions (continued)

Pin Name	Description	Pin Number	Power
Power, Ground, and Reserved Pins			
+5V	This pin is connected to the system's 5-volt power supply. In systems where 5 volts is not available, this pin can be connected to the system's 3.3-volt supply (but 5-volt-only PC Cards will not be supported).	127	PWR
CORE_VDD	This pin provides power to the core circuitry of the CL-PD6730. It must be connected to 3.3-volt power supply.	134	PWR
CORE_GND	All CL-PD6730 ground pins should be connected to system ground.	26	GND
RING_GND	All CL-PD6730 ground pins should be connected to system ground.	14, 28, 44, 57, 129, 146, 163, 177, 193	GND
RESERVED1	This pin is reserved. For future expansion, connect this pin to GNT# on the PCI bus.	2	
RESERVED2	This pin is reserved. For future expansion, connect this pin to REO# on the PCI bus.	3	
RESERVED3	This pin is reserved. For future expansion, connect this pin to LOCK# on the PCI bus.	58	

2.9 PCI0643 PCI E-IDE Controller

2.9.1 Features

- Capable of 16 MB/second transfer rates in DMA mode - up to 20 MB/second in PIO mode
- Supports bus master DMA at 133 MB/second PCI burst rate
- Support PCI DMA transfers for both DMA-capable and PIO-only drives
- Fully supports ATAPI DMA/PIO transfers
- 2 channels - supports up to 4 IDE drives
- Surpasses and supports Enhanced IDE Mode 3, Mode 4 and propose Mode 5 timing from the widest range of disk drive manufacturers
- Supports multi-word and single-word DMA modes 0, 1 and 2
- Fully supports the latest PCI-IDE specification and all the Plug-and-Play (PnP) specifications.
- Supports Windows 95, Windows NT 3.1 and 3.5 (Daytona), OS/2
- CMD's complete set of 32-bit drivers handle both DMA and PIO
- Fully compatible with the latest PCI, PCI IDE, ATA-2, Enhanced IDE, Fast IDE, ATAPI, plug and play, and ATA-2 Power Management Feature Set
- Fully supports all ATAPI-compatible devices, including CD-ROM, tape, MO, and other devices
- Fully supports legacy (IRQ 14 and 15)
- Hardware and software mode switching and chip enable/disable capabilities
- Programmable read-ahead and write-back buffers enhance transfer rates
- Fully compatible with all major operating systems
- 100-pin PQFP

2.9.2 Pin Diagram

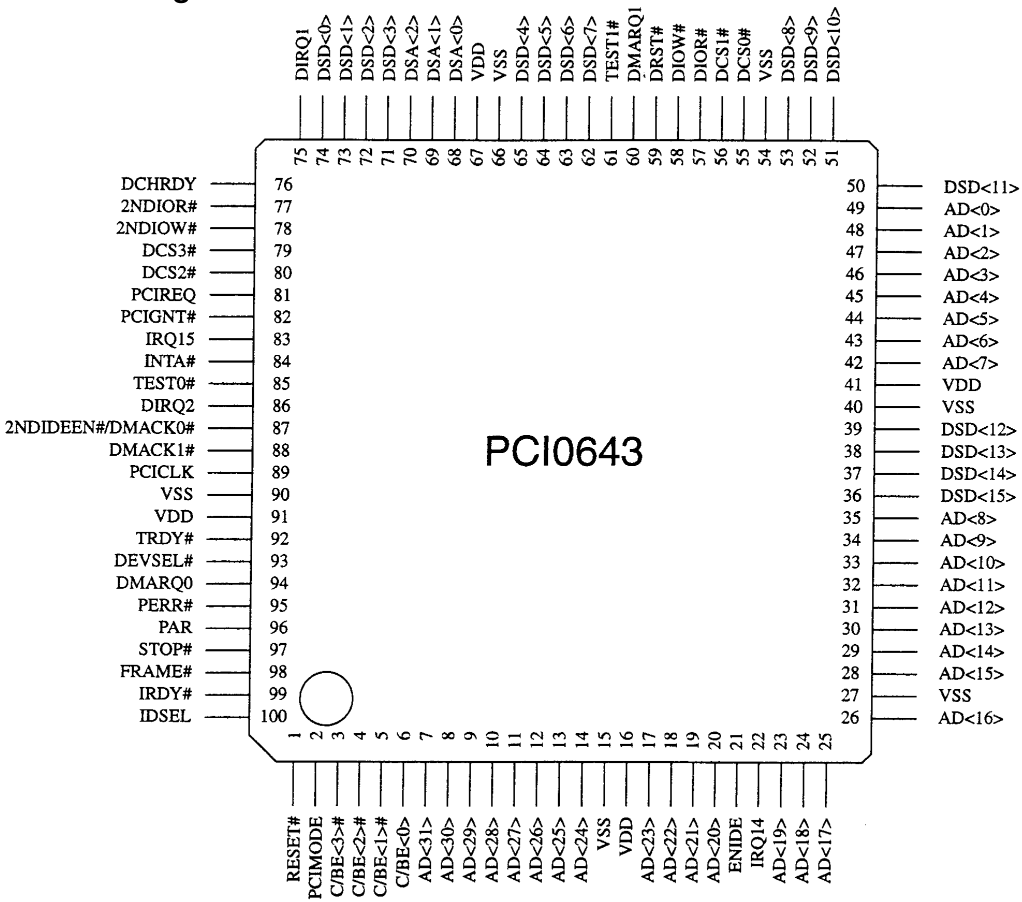


Figure 2-19 PCI0643 Pin Diagram

2.9.3 Signal Descriptions

Table 2-15 PCI0643 Signal Descriptions

Signal	Pin	Type	Description
2NDIDEEN#/ DAMCK0	87	B/T	**Secondary IDE Channel Enable and DMA Request Acknowledge 0** This signal is used in response to DMARQ0 to wither acknowledge that data has been accepted, or that data is available. At power-up, the state of this signal is used to enable or disable the secondary channel.
2NDIOR#	77	T/O	**Secondary Channel Disk I/O Read.** This is an active low output which enables data to be read from the drive. The duration and repetition rate of DIOR# cycles is determined by PCI0643 programming. DIOR# is driven high when inactive.
2NDIOW#	78	T/O	**Secondary Channel Disk I/O Write** This is an active low output that enables data to be written to the drive. The duration and repetition rate of DIOW# cycles is determined by PCI0643 programming. DIOW# is driven high when inactive.
AD[31:0]	7-14, 17-20, 23-26, 28-35, 42-49	B/T	**Address and Data.** Address and data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the clock cycle in which FRAME# is asserted. During the address phase, AD[31:0] contain a physical address (32 bits). For I/O, this is a byte address. For configuration and memory, it is a Dword address. During data phases, AD[31:24] contain the least significant byte (lsb) and AD[31:24] contain the most significant byte (msb). Write data are stable and valid when TRDY# is asserted. Data are transferred during those clocks where both IRDY# and TDY# are asserted.
C/BE[3:0]#	3-6	B/T	**Byte Enable bits 0 through 3.** These form the host CPU address bus. These inputs are active low and specify which bytes are valid for host read/write data transfers.
DMACK1#	88	B/T	This signal normally is used in response to DMARQ1 to either acknowledge that data has been accepted.
DCHRDY	76	I	**Disk Ready.** This is an active high input that indicates that the IDE disk drive has completed the current command cycle. A 1KΩ pull-up resistor is recommended.
DCS0#	55	O	**Disk Chip Select 0.** Drive chip select for 1Fx.
DCS1#	56	O	**Disk Chip Select 1.** Drive chip select for 3F6.
DCS2#	80	O	**Disk Select 2.** This is used to select the second IDE port command registers in the drive.
DCS3#	79	O	**Disk Select 3.** This is used to select the second IDE port auxiliary register.

Table 2-15 PCI0643 Signal Descriptions (continued)

Signal	Pin	Type	Description
DEVSEL#	93	S/T/S	**Device Select.** When this signal is actively driven, it indicates that the driving device has decoded its address as the target of the current access. As an input, it indicates to a master whether any device on the bus has been selected.
TEST1#	61	I	This pin is used with TEST0 when PCIMODE=0 to select different DC tests for this chip.
DIOR#	57	T/O	**Primary Disk I/O Read.** An active low output that enables the data to be read from the drive . The duration and repetition rate of the DIO# cycles is determined by the PCI0643 programming. DIOR# is driven high when inactive.
DIOW#	58	T/O	**Primary Disk I/O Write.** This is an active low output that enables data to be written to the drive. The duration and repetition rate of DIOW# cycles is determined by PCI0643 programming. DIOW# is driven high when inactive.
DIRQ1	75	I	**Disk Interrupt.** This pin is an input to the PCI066 that generates the IRQ14 output. DINT is asserted low, then high by the drive at the beginning of a block transfer. This input should have a external 1KΩ resistor and a 47pF capacitor pull down connected to it.
DIRQ2	86	I	**Disk Interrupt.** Input for the secondary IDE port. It is used to generate the IRQ15 output. DIRQ2 is asserted low then high by the drive at the beginning of a block transfer. This input should have a external 1KΩ resistor and a 47pF capacitor pull down connected to it.
DMARQ0	94	I	**DMA Request 0.** This signal is used in a handshake manner with DMACK0#, and should be asserted high by the primary drive when it is ready to transfer data to or from the host.
DMARQ1	60	I	**DMA Request 1.** This signal is used in a handshake manner with DMACK1#, and should be asserted high by the primary drive when it is ready to transfer data to or from the host.
DRST#	59	O	**Disk Reset.** This is an active low output which signals the IDE drive(s) to initialize its control registers. DRST# is a buffered version of the RESET# input and connects directly to the ATA connector.
DSA2 DSA1 DSA0	70, 69, 68	O, B/T, O	**Disk Address bits from 0 through 2.** These are normally outputs to the ATA connector for register selection in the drive(s). These signals are decoded from the A2 and C/BE[3:0] inputs. DSA[1] is also sampled as inputs on the falling edge of RESET#. All of these pins have internal pull-up resistors. 2.2KΩ resistors are recommended where pull-downs are required.

Table 2-15 PCI0643 Signal Descriptions (continued)

Signal	Pin	Type	Description
DSD[15:0]	36-39, 50-53, 62-65, 71-74	B/T	**Disk Data bits 0 through 15.** These are 16-bit bidirectional data bus that connects to the IDE drive(s). DSD[7:0] define the lowest data byte while the DSD [15:8] define the most significant data byte. The DSD bus is normally in a high-impedance state and is driven by the PCI0643 only during the DIOW# command pulse.
ENIDE	21	I	**Enable IDE.** This is an active high input that enables the PCI0643's default mode disk operation following reset. When set to low, the PCI0643 is disabled following reset. This mode allows software to scan for system hardware and enable the PCI0643 via the PCME register (index 4). When left floating or pulled high, the PCI0643 is enabled and cannot be disabled via software.
FRAME#	98	S/T/S	**Cycle Frame.** This is driven by the current master to indicate the beginning and the duration of an access. FRAME# is asserted to indicate that a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is de-asserted, the transaction is in the final data phase.
IDSEL#	100	I	**Initialization Device Select.** This pin is used as a chip select during configuration read and write transactions.
INTA#	84	O/D	**Interrupt A.** This is used to request an interrupt in PCI IDE Native Mode. INTA# is tristated when both IDE port are in Legacy Mode.
IRDY#	99	S/T/S	**Initiator Ready.** This indicates the initializing agent's (bus master's) ability to complete the current data phase of the transaction. This signal is used with TRDY#. A data phase is completed on any clock when both IRDY# and TRDY# are sampled asserted. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
IRQ14	22	T/O	**IRQ14.** This is used to request an interrupt in PCI IDE legacy Mode (for PC-AT compatibles). IRQ14 is tristated when IDE port 0 is in Native Mode.
IRQ15	83	T/O	**IRQ15.** This is used to request an interrupt in PCI IDE legacy Mode (for PC-AT compatibles). IRQ15 is tristated when IDE port 1 is in Native Mode.
PAR	96	B/T	**Parity.** PAR is even parity across AD[31:0] and C/BE[3:0]#. Parity generation is required by all PCI agent. PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. (PAR has the same timing as ad[31:0] but delayed by one clock).

Table 2-15 PCI0643 Signal Descriptions (continued)

Signal	Pin	Type	Description
PCICLK	89	I	**Clock Signal.** This signal provides timing for all transaction on PCI and is an input to every PCI device. All other PCI signals, except RESET# and IRQ, are sampled on the rising edge of PCICLK, and all other timings with respect to this edge.
PCIGNT#	82	I	**PCI Grant.** This signal indicates to the agent that access to the PCI bus has been granted.
PCIMODE	2	I	**PCI Mode.** This is et to high when chip is used in PCI bus.
PCIREQ#	81	T/O	**PCI Request.** This signal indicates to the arbiter that this agent desires use of the PCI bus.
PERR#	95	S/T/S	**Pulsed Error.** Error may be pulsed active by an agent that detects a parity error. PERR# can be used by any agent to signal data corruption. However, on detection of a PERR# pulse, the central resource may generate a non-Maskable interrupt to the host CPU which often implies that the system is unable to continue operation once an error processing is completed.
RESET#	1	I	**Reset.** This is an active high input that is used to set the internal registers of the PCI0643 to their initial state. RESET# is typically the system power-on reset signal as distributed on the PCI bus.
STOP#	97	S/T/S	**Stop.** This indicates that the current target is requesting the master to stop the current transaction.
TEST0	85	I	**TEST0.** This pin is used with DIOCS16# when PCIMODE-0 to select different DC tests for this chip.
TRDY#	92	S/T/S	**Target Ready**. This indicates that the target agent's ability to complete the current data phase of the transaction. TRDY# is used with IRDY#. A data phase is completed on any clock when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD(31:0). During a write, it indicates the target is prepared to accept data.
VDD	16, 41, 67, 91	I	**3V Positive Power Supply Input.**
VSS	15, 27, 40, 54, 66, 90	I	**Ground Reference Input.**

2.10 Ambit T62.036.C DC-DC Converter

This T62.036.C DC-DC converter supplies multiple DC(5V, 3,3V, 12V) output to system, and also supplies the battery charge current (0~3.5A). The total inputs from the notebook would be limited by the total output of 65 watts maximum.

2.10.1 Pin Diagram

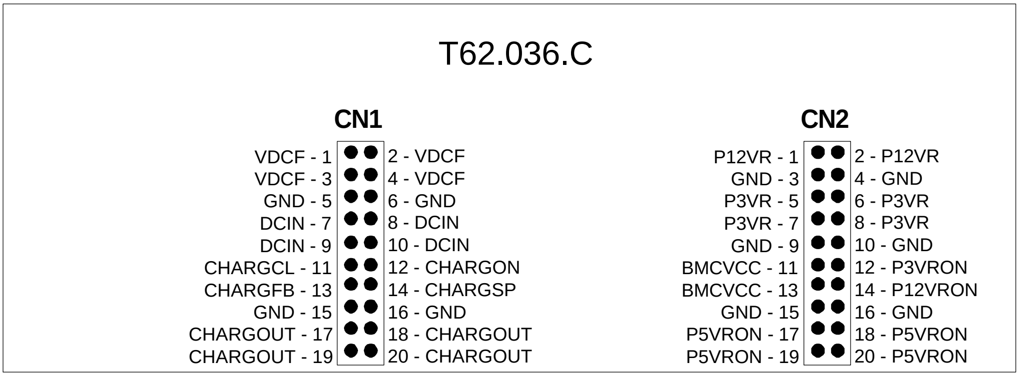


Figure 2-20 T62.036.C Pin Diagram

2.10.2 Pin Descriptions

Table 2-16 T62.036.C Pin Descriptions

Pin Name	Pin Type	Pin No.	Description
CN1 signals			
VDCF	I	1, 2, 3, 4	18VDC input from battery.
DCIN	I	7, 8, 9, 10	7~19VDC input from AC adapter.
CHARGCL	I	11	Enables Charger output. This input is driven by an open drain signal to set the charging current limit to a high (3 .5A max.) or low (2A). The lower limit is set when the signal is low (switch on). The system will generally set this signal low when the battery has been discharged to a low level. The battery current sensor is built into the charger circuitry. The resistance of the drain switch is less than 1KΩ. Note, this signal sets the limit value of the charging current. The CHARGFB and CHARGSP signals may restrict the charging current to a lower level.

Table 2-16 T62.036.C Pin Descriptions (continued)

Pin Name	Pin Type	Pin No.	Description
CN1 signals (continued)			
CHARGON	I	12	This is a logic level signal, active high to enable the adapter current output. This signal allows the system board to turn off the charger output whenever the battery pack reports unsafe conditions such as over temperature, error or no communication. It may be used in response to any other detectable unsafe system conditions ±1uA maximum loading.
CHARGFB	I	13	This signal is provided by a current sensor in the system to indicate the current drawn from the AC adapter or other power source such as docking station power supply. This level is 2 Amps per volt nominal. The source impedance is less than 1KΩ.
CHARGSP	I	14	Analog input from the system board to limit the total current consumed by the system from the AC adapter. This signal shall be compared by the module with the CHARGFB from the system mother board and the battery charger output current adjusted until CHARGFB does not exceed CHARGSP. The system board generates CHARGESP in conjunction with a ID resistor embedded in the LCD cable. The scale is 2 amps per volt. The source impedance is less than 2KΩ. Note: The battery charger output may be reduced below the level of CHARGESP by the battery charger current limit signal CHARGECL.
GND	GND	15, 16	Ground
CHRGOUT	I	17, 18, 19, 20	Battery charger current source output at 3.5A max. The output current is controlled by two control signals which limit the battery charging current and AC adapter output current. The output voltage is limited to 13.2V~13.5V.
CN2 signals			
P12VR	O	1, 2	+12V output, 0~0.5A.
GND	GND	3, 4, 15, 16	Ground
P3VR	O	5, 6, 7, 8	+3.3V output, 0~3A.
BMCVCC	O	11, 13	+5V output, 0~0.5A. Used for resuming from suspend-to-memory mode.
P3VRON	O	12	Enables P3VR. Logic level, Active high, +/-luA max loading
P5VRON	O	14	Enables PSVR. Logic level, Active high, +/-luA max loading
P5VR	O	17, 18, 19, 20	+5V output, 0~2.5A.

2.11 Ambit T62.039.C/T62.055.C DC-AC Inverter

This notebook has two kinds of DC-AC inverter. One(T62.039.C) is designed for HITACHI LMG9930ZWCC and TX30D01VC1CAA LCD use, the other(T62.055.C) is for IBM ITSV50D LCD use.

2.11.1 Pin Diagram

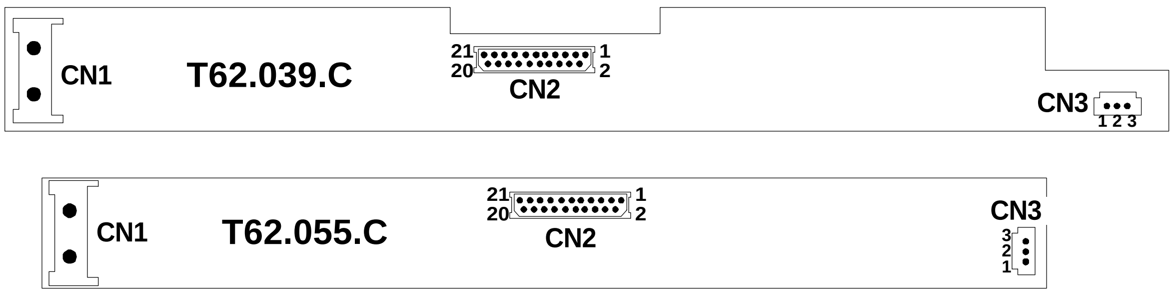


Figure 2-21 T62.039.C/T62.055.C Pin Diagram

2.11.2 Pin Descriptions

Table 2-17 T62.039.C/T62.055.C Pin Descriptions

Pin Name	Pin Type	Pin No.	Descriptions
CN1 connector signals			
Vhi Vlo	O	1 2	This is the High voltage side of the Lamp. (The shorter wire to lamp connects to this output. T62.039.C / T62.055.C Max lamp start voltage(Vrms): 1200 / 1300 Typical lamp run voltage @25°C(Vrms): 520 / 650 Min open circuit voltage (Vrms): 1300 / 1100 Max open circuit voltage(Vrms): 1600 / 1500
CN2 connector signals			
GND	GND	1, 6	This the return signal for the input power and control signals and is an extension of the system ground.
CNTADJ	O	2, 9	Contrast adjustment (reserved)
DCIN	I	3, 4, 5	This is the input DC voltage to supply the operating power. Max value: 19VDC Min value: 7 VDC
BRTADJ	O	7	This is an analog signal in the range of 0 to 3 volts to control the lamp current. Vbrite = 1 volt, Lamp current = 50%±10% of Max. Vbrite = 3volts, Lamp current = Max = 4.5mA

Table 2-17 T62.039.C/T62.055.C Pin Descriptions (continued)

Pin Name	Pin Type	Pin No.	Descriptions
CN1 connector signals (continued)			
PANEL_ON	I	8	A control pin to control on/off lamp. This input enable the inverter operation (Lamp On) when high and disables the inverter when low. This signal is output from a 3.3V CMOS device. Max loading = 100uA Logic Low = 0.8 volts Max. Logic High =1.8 volts Min.
PWRLED	O	12	This signal is an open collector sink signal to drive LED1. The LED current is limited by a series resistor of 1KΩ.
BATTLED	O	13	This signal is an open collector sink signal to drive LED2. The LED current is limited by a series resistor of 1KΩ.
BMCVCC	O	14	This a 5 volt supply for powering the LEDs. It should not be used for any other purpose.
ADVDD	O	18	This is a 5 volt power line for the analog circuits and display LEDs on the inverter board.
AUDGND	GND	19, 20	This is the return ground for the microphone circuit. It should not be connected to VGND or other circuit on the inverter board.
MIC_OUT	O	21	This is the output of the microphone preamplifier circuit.
N.C.	-	10, 11, 15, 16, 17	Non-connected.
CN3 connector signals			
MIC-CON	I	1	Microphone input
N.C.	-	2	Non-connected.
AUDGND	GND	3	This is the return ground for the microphone circuit. It should not be connected to VGND or other circuit on the inverter board.

Chapter 3

BIOS Setup Information

The notebook has a BIOS (Basic Input/Output System) setup utility that allows you to configure the notebook and its hardware settings. This chapter tells how to use the Setup utility and describes each parameter item in the setup screens.

3.1 When to Use Setup

The notebook is already correctly configured for you and you do not need to run Setup. If you make any changes to the notebook or you receive an Equipment Configuration Error message after you turn on the notebook, you may need to run Setup. Run Setup also if you want to do any of the following:

- Check the system configuration
- Change the system date, time or speed
- Add or change the location of the external mouse
- Change the system startup sequence
- Set the power-saving suspend mode type
- Set or change resume options
- Set, change, or remove a system password

The system configuration values reside in the battery-powered CMOS RAM.

3.2 Entering Setup

Press **Fn-F2** to enter Setup. The BIOS Utility main screen displays.

```
                         BIOS Utility

                      About My Computer
                     System Configuration
                     Power Saving Options
                       System Security
                  Reset to Default Settings

   ↑↓←→ = Move Highlight Bar, ↵ = Select, Esc = Exit
```

There are five main menu items:

- About My Computer
- System Configuration
- Power Saving Options
- System Security
- Reset to Default Settings

Press ↑, ↓, ← or → to move from one menu item to another and press **Enter** to enter the selected menu. Press **Esc** to exit Setup.

3.3 About My Computer

About My Computer gives you clear-cut information about your notebook PC. The following screen is the first of two pages in this section.

```
                         About My Computer            Page 1/2

  System Architecture : MARS 1996-1997
          System BIOS : BIOS V2.0
            System ID : VGA010602, KBC010607, SMC010023, SMM010210
            Processor : Pentium / 133MHz
          Coprocessor : Integrated
  Internal Cache (L1) :  16KB, Enabled
  External Cache (L2) : 256KB, Enabled
         Total Memory :  16 MB
               Bank A :   0 MB
               Bank B :  16 MB
  Graphics Controller : 128-bit Graphics Acceleration
       Display Output : TFT, 800x600
         Hard Drive 0 : Hard Disk,  1160MB
         Hard Drive 1 : CD-ROM
       Floppy Drive A : 1.44 MB 3.5-inch
       Floppy Drive B : None

 PgDn/PgUp = Move Screen, Esc = Exit
```

Press **PgDn** to view the second page.

```
                         About My Computer            Page 2/2

  Expansion Peripherals
        PCMCIA Slot 0 : None
        PCMCIA Slot 1 : None
        Parallel Port : 378h, IRQ7
          Serial Port : 3F8h, IRQ4
                 IrDA : 2F8h, IRQ3
                Modem : 3E8h, IRQ 10, 33.6 kbps, V.34, DSVD
           AC Adapter : None
         Main Battery : 60W Li-Ion

   Onboard Audio
         Base Address :  240h
     MPU Base Address :  300h
          IRQ Setting : IRQ 5
          DMA Channel : DMA 0

 PgDn/PgUp = Move Screen, Esc = Exit
```

Press **PgUp** to return to the first page. To return to the main screen, press **Esc**.

ABOUT MY COMPUTER ITEMS

These screens display the current status of the notebook and its peripherals. The items in this screen are not user-configurable.

Table 3-1 About My Computer Item Descriptions

Item	Description
System	
System Architecture	System architecture information
System BIOS	BIOS manufacturer and version
System ID	ID information on major components
Processor	Processor type and speed
Coprocessor	Coprocessor type
Internal Cache (L1)	Internal cache size and whether it is enabled or not
External Cache (L2)	External cache size and whether it is enabled or not
Total Memory	Total memory size
Bank A	Bank A memory module size, type and speed
Bank B	Bank B memory module size, type and speed
Graphics Controller	Graphics controller type
Display Output	Display type and resolution
Hard Drive 0	IDE 0 drive type and size (hard disk)
Hard Drive 1	IDE 1 drive type (CD-ROM or other IDE drives)
Floppy Drive A	Floppy drive A type
Floppy Drive B	Floppy drive B type
Expansion Peripherals	
PCMCIA Slot 0	Card presence in slot 0 (detected by the socket service)
PCMCIA Slot 1	Card presence in slot 1 (detected by the socket service)
Parallel Port	Parallel port base address and IRQ
Serial Port	Serial port base address and IRQ
IrDA	Infrared port base address and IRQ
Modem	Modem address and other information
AC Adapter	Connected AC adapter information
Main Battery	Installed battery type information
Onboard Audio	
Base Address	Audio base address
MPU Base Address	Audio MPU-401 base address
IRQ Setting	Audio IRQ setting
DMA Channel	Audio DMA channel

3.4 System Configuration

The following screen is the basic system configuration screen.

```
                    Basic System Configuration           Page 1/1

Current Date ---------------- [09/16/96]
Current Time ---------------- [16:30:35]

Diskette Drive A ------------ [1.44 MB 3.5-inch]
Diskette Drive B ------------ [      None      ]

                                           Cylinder  Head  Sector
Hard Disk 0 (1160 MB) ------- [Auto]           2358   16      63
Hard Disk 1 (   0 MB) ------- [Auto]              0    0       0

Num Lock After Boot --------- [Disabled]
LCD Expansion Mode ---------- [Disabled]

↑↓ = Move Highlight Bar, ←→ = Change Setting
PgDn/PgUp = Move Screen, F1 = Help, Esc = Exit
```

Press ↑ or ↓ to move from one parameter to another, and ← or → to change parameter settings.

Most of the parameters are self-explanatory, but you can press **F1** to get help on the selected parameter. Press **Esc** to exit the screen and return to the main menu.

3.4.1 Date and Time

The current date is in MM/DD/YYYY format. The current time is in HH:MM:SS format. The system uses a 24-hour clock which means, for example, that 6:25:50 PM appears as 18:25:50.

3.4.2 Diskette Drives

The default setting for Diskette Drive A is **[1.44 MB 3.5-inch]** and refers to the floppy drive whether it is installed in the module bay or connected externally via the parallel port. Diskette Drive B by default is set to **[None]**, and is only enabled if two floppy drives are connected to the notebook.

3.4.3 Hard Disks

The Hard Disk 0 parameter is reserved for the hard disk. With this parameter set to **[Auto]**, the BIOS automatically detects the hard disk parameters and displays the formatted capacity in the parentheses right after the Hard Disk 0 parameter heading. It also displays the cylinder, head and sector values of the hard disk. Advanced hard disk settings are auto-configured by Setup for optimum drive performance.

You can also choose to key-in the drive parameters by setting Hard Disk 0 to **[User]**. To determine your drive parameters, check the data found on your hard disk or supplied in the hard disk vendor documentation. We suggest that you set this parameter to **[Auto]** to allow the BIOS to auto-detect the drive parameters at each boot-up.

The Hard Disk 1 parameter is used when a CD-ROM drive module or future IDE drive option is installed in the module bay. The default setting for both parameters is **[Auto]**.

3.4.4 Num Lock After Boot

When enabled, Num Lock turns on after boot and the embedded keypad acts as a numeric keypad. The default setting is **[Disabled]**.

3.4.5 LCD Expansion Mode

When enabled, the LCD screen shows in expanded mode. By default, this parameter is set to **[Disabled]**.

For advanced users, the System Configuration section has two hidden pages called Advanced System Configuration that allow you to view and configure more technical aspects of the notebook.

The notebook's BIOS configuration is already tuned for optimum performance and you do not need to access these screens. If you do not fully understand the items in these special screens, do not attempt to change their values.

If you happen to change the values and decide you want to return the previous values, select the Reset to Default Settings in the main menu to restore all default values.

To access the Advanced System Configuration screens, press **F8** from the main menu. Then select System Configuration to enter the System Configuration screens. Note that the pages in this section now total three. Press **PgDn** to access the first of two hidden screens.

```
                  Advanced System Configuration        Page 2/3

Internal Cache(CPU Cache) -------- [Enabled]
    Cache Scheme ----------------- [ Write Back ]
External Cache ------------------- [Enabled]

Enhanced IDE Features Hard Disk 0
    Hard Disk Size > 504MB ------- [DOS/Win3.x/Win95]
    Multiple Sectors Read/Write -- [   Auto   ]
    Advanced PIO Mode ------------ [ Auto ]
    Hard Disk 32-Bit Access ------ [  Auto  ]

Enhanced IDE Features Hard Disk 1
    Hard Disk Size > 504MB ------- [DOS/Win3.x/Win95]
    Multiple Sectors Read/Write -- [   Auto   ]
    Advanced PIO Mode ------------ [ Auto ]
    Hard Disk 32-Bit Access ------ [  Auto  ]

↑ ↓ = Move Highlight Bar, → ← = Change Setting
PgDn/PgUp = Move Screen, F1 = Help, Esc = Exit
```

Press **PgDn** again to access the next hidden screen.

```
                  Advanced System Configuration        Page 3/3

Onboard Communication Ports
    Serial Port Base Address --- [3F8h, IRQ4]
    IrDA Base Address ---------- [2F8h, IRQ3]
    Modem Base Address --------- [  3E8h  ]
        IRQ Setting ------------ [10]
    Parallel Port Base Address - [378h, IRQ7]
        Operation Mode --------- [  Standard and Bidirectional   ]
            ECP DMA Channel ---- [-]

Onboard Audio ------------------ [Enabled ]
    Base Address --------------- [240h]
    MPU Base Address ----------- [300h]
    IRQ Setting ---------------- [ 5]
    DMA Channel ---------------- [0]

Reset PnP Resources ------------ [No ]

↑ ↓ = Move Highlight Bar, → ← = Change Setting
PgDn/PgUp = Move Screen, F1 = Help, Esc = Exit
```

3.4.6 Internal Cache

Internal cache refers to cache built into the CPU. When enabled, this setting boosts system performance. It is also called CPU cache or L1 (level one) cache. The default setting is **[Enabled]**.

The Cache Scheme parameter accepts two values:

- **Write Back**
- **Write Through**

which determines how the system uses the internal cache. The default setting is **[Write Back]**.

3.4.7 External Cache

External cache greatly increases system performance by lessening the load of main memory. It is also called L2 (level 2) cache. The default setting is **[Enabled]**.

3.4.8 Enhanced IDE Features

The Enhanced IDE Features section includes four parameters for optimizing hard disk performance. These performance features depend on drive support. Newer drives support most or all of these features.

As much as possible, set these parameters to [Auto] (when the option to do so is available). This allows the notebook to use the hard drive with the highest possible performance level.

3.4.8.1 Hard Disk Size > 504MB

If your hard disk size is greater than 504MB and you are operating in a DOS-based environment, this parameter should be set to **[DOS/Win3.x/Win95]**. If you operate in NetWare, UNIX and Windows NT environments, set this parameter to **[Others]**. The default setting is **[DOS/Win3.x/Win95]**.

3.4.8.2 Multiple Sectors Read/Write

This parameter enhances hard disk performance by reading/writing more data at once. The available values include:

- **Auto**
- **16 sectors**
- **8 sectors**
- **Disabled**

The highest value, 16 sectors, may not give you the best performance every time, because hard disks behave differently. The default setting, **[Auto]**, allows the system to adjust itself to the optimum read/write setting.

3.4.8.3 Advanced PIO Mode

Advanced PIO (Programmed Input/Output) Mode enhances drive performance by optimizing the hard disk timing. The available values include:

- **Auto**
- **Mode 0**

The default setting is **[Auto]**.

3.4.8.4 Hard Disk 32-Bit Access

This parameter allows your hard disk to perform 32-bit access, an increase from the original 16-bit access. The available values include:

- **Auto**
- **Disabled**

The default setting is **[Auto]**.

3.4.9 Onboard Communication Ports

The Onboard Communication Ports section includes settings for the serial and parallel ports on the notebook. The addresses in this screen are all expressed in hexadecimal.

Resource conflicts are prevented by not allowing you to set the same IRQ and address values for different devices.

3.4.9.1 Serial Port Base Address

This parameter accepts the following values:

- **[3F8h, IRQ 4]**
- **[2F8h, IRQ 3]**
- **[3E8h, IRQ 4]**
- **[2E8h, IRQ 3]**
- **[Disabled]**

The default setting is **[3F8h, IRQ 4]**.

3.4.9.2 IrDA Base Address

This parameter accepts the following values:

- **[2F8h, IRQ 3]**
- **[Disabled]**

The default setting is **[2F8h, IRQ 3]**.

3.4.9.3 Modem Base Address and IRQ Setting

MODEM BASE ADDRESS

This parameter accepts the following values:

- **[3E8h]**
- **[2E8h]**
- **[Disabled]**

The default setting is **[3E8h]**.

IRQ SETTING

The IRQ Setting parameter for the modem accepts 3, 4, 5, 7 or 10 as its value. The default setting is **[10]**.

3.4.9.4 Parallel Port Base Address, Operation Mode and ECP DMA Channel

PARALLEL PORT BASE ADDRESS

The Parallel Port Base Address parameter accepts the following values:

- **[378h, IRQ 7]**
- **[3BCh, IRQ 7]**
- **[278h, IRQ 5]**
- **[Disabled]**

The default setting is **[378h, IRQ 7]**.

OPERATION MODE

The Operation Mode parameter for the parallel port accepts the following:

- **[Standard and Bi-directional]**
- **[Enhanced Parallel Port (EPP)]**
- **[Extended Capabilities Parallel Port (ECP)]**

Enhanced Parallel Port (EPP) provides greater throughput by supporting faster transfer times and a mechanism that allows the host to address peripheral device registers directly. Extended Capabilities Port (ECP) supports a 16-byte FIFO (first in, first out) which can be accessed by host DMA cycles and PIO cycles.

The default setting is **[Standard and Bi-directional]**.

ECP DMA CHANNEL

The ECP DMA Channel parameter lets you set the DMA channel used for ECP mode. You are required to set a value for this parameter if you select ECP as your parallel port operation mode. It accepts 1 or 3 as its value.

3.4.10 Onboard Audio

This parameter lets you enable or disable the onboard audio functionality of the notebook. This section also includes settings for onboard audio. The default setting is **[Enabled]**.

3.4.10.1 Base Address

This parameter accepts the following values:

- **[220h]**
- **[230h]**
- **[240h]**
- **[250h]**

The default setting is **[240h]**.

3.4.10.2 MPU Base Address

This parameter accepts the following values:

- **[300h]**
- **[310h]**
- **[320h]**
- **[330h]**

The default setting is **[300h]**.

3.4.10.3 IRQ Setting

This parameter accepts 10, 7, 5 or 9 as its value. The default setting is **[5]**.

3.4.10.4 DMA Channel

This parameter accepts 0, 1 or 3 as its value. The default setting is **[0]**.

3.4.11 Reset PnP Resources

The system resources are already properly configured. If resource conflicts should arise, set this parameter to [**Yes]** to reset the PnP resources and re-do allocation. The BIOS automatically sets this to **[No]** afterwards.

The default setting is **[No]**.

3.5 Power Saving Options

The following screen is the power saving options screen.

```
                      Power Saving Options              Page 1/1

When Lid is Closed ------------------ [ Suspend to Disk ]
Suspend to Disk on Critical Battery - [Enabled ]

Display Always On ------------------- [Disabled]
Internal Speaker -------------------- [Enabled ]
External Mouse Location ------------- [PS/2]
Internal Modem ---------------------- [Power-On]

Resume On Modem Ring ---------------- [OFF]
Resume On Schedule ------------------ [OFF]
    Resume Date --------------------- [09/16/96]
    Resume Time --------------------- [16:30:35]

↑ ↓ = Move Highlight Bar, → ← = Change Setting
PgDn/PgUp = Move Screen, F1 = Help, Esc = Exit
```

Press ↑ or ↓ to move from one parameter to another, and ← or → to change parameter settings.

Most of the parameters are self-explanatory, but you can press **F1** to get help on the selected parameter. Press **Esc** to exit the screen and return to the main menu.

3.5.1 When Lid is Closed

The notebook's lid switch acts as its power switch. Simply put, opening the display wakes up the notebook; closing the display puts it to sleep. The When Lid is Closed parameter determines which suspend mode the notebook enters when the display is closed. There are two settings for this parameter:

- **Suspend to Memory**
- **Suspend to Disk**

With this parameter set to **[Suspend to Memory]**, the notebook enters suspend-to-memory mode (saving all data into memory) when you close the display or press the suspend hot key **Fn-Esc** (Z^z). The notebook wakes up when you open the display or press any key.

With the parameter set to **[Suspend to Disk]**, the notebook enters suspend-to-disk mode (saving all data into the hard disk) when you close the display. The notebook wakes up when you open the display again.

If an external monitor is connected to the notebook, the notebook will not enter suspend mode if you close the display. To enter suspend mode, disconnect the monitor plug, open the display and close the display again.

The Sleep Manager automatically creates a suspend-to-disk file when it is run. If the file becomes invalid, the notebook will be unable to enter suspend-to-disk mode, and enters suspend-to-memory mode.

3.5.2 Suspend to Disk on Critical Battery

With this parameter set to **[Enabled]**, the notebook enters suspend-to-disk mode when the battery becomes critically-low. The default setting is **[Enabled]**.

3.5.3 Display Always On

This parameter lets you specify whether the display is always on or not. When enabled, the screen will not blank. The default setting is **[Disabled]** to save power.

3.5.4 Internal Speaker

This parameter lets you turn the internal speaker on and off. The default setting is **[Enabled]**.

You can also do this by pressing the speaker on/off toggle hot key **Fn-F7**. Pressing this hot key changes this parameter setting in Setup.

3.5.5 External Mouse Location

This parameter lets you specify the location of your mouse or similar pointing device. Four settings are available for this parameter:

- **COM 2**
- **COM 1**
- **PS/2**

Since the touchpad is a PS/2-compatible device, the default setting is **[PS/2]**. If you connect an external PS/2 mouse or similar pointing device, you do not need to change the setting. If, however, you want to use an external serial mouse, change this parameter setting accordingly.

3.5.6 Internal Modem

For models with an internal modem, set this parameter to **[Power-On]** when you are using the internal modem. If you are not actively using the internal modem, you can set this parameter to **[Power-Off]** to conserve power. The default setting is **[Power-On]**.

3.5.7 Resume On Modem Ring

You can set the notebook to resume from suspend-to-memory mode upon detection of a specific number of modem rings, ranging from 1 to 7.

Enabling this option overrides the suspend-to-disk function.

3.5.8 Resume On Schedule

When enabled, the notebook resumes from suspend-to-memory mode at the specified Resume Date and Resume Time settings.

Enabling this option overrides the suspend-to-disk function.

3.5.9 Resume Date / Resume Time

The Resume Date and Resume Time parameters let you set the date and time for the resume operation. The date and time fields take the same format as the System Date and Time parameters in the System Configuration screen.

If you set a date and time prior to the time of suspend, this field is automatically disabled. A successful resume occurring from a date and time match also automatically disables this field.

3.6 System Security

The following screen is the system security screen.

If a password is currently present, the system prompts you to input the password before entering the System Security screen.

```
                        System Security                Page 1/1

Supervisor Password ------------ [ None ]
User Password ------------------ [ None ]

Disk Drive Control
    Diskette Drive ------------- [  Normal   ]
    Hard Disk Drive ------------ [  Normal   ]
    Start Up Sequences --------- [     A: then C:     ]

Flash New BIOS ----------------- [Disabled]

↑↓=Move Highlight Bar, →←=Change Setting, F1=Help, Esc=Exit
```

Press ↑ or ↓ to move from one parameter to another, and ← or → to change parameter settings.

Most of the parameters are self-explanatory, but you can press **F1** to get help on the selected parameter. Press **Esc** to exit the screen and return to the main menu.

3.6.1 Supervisor and User Passwords

The supervisor and user passwords both prevent unauthorized access to the notebook. When these passwords are present, the notebook prompts for the user or supervisor password during system boot-up and resume from suspend. The supervisor password also gives full access to Setup. The user password give limited access to Setup.

Setup requires the supervisor password to be set prior to setting the user password.

If you enter Setup using the user password, you cannot modify the supervisor password and certain BIOS settings.

SETTING A PASSWORD

To set a password:

1. Select the desired password (Supervisor or User) to set or edit, and press ← or →. The password prompt (a key) appears:



2. Enter a password.

   The password may consist of up to eight characters which do not appear on the screen when you type them. After typing your password, press **Enter**. Another password prompt appears:



3. Retype your password and press **Enter** to verify your first entry.

   After setting a password, the notebook sets this parameter to **`[Present]`**. The next time you boot the notebook, resume from suspend mode, run the Setup utility or unlock system resources, the password prompt appears. Key in the appropriate password (Supervisor or User). The system asks for your password input until you enter the correct password.

If you forget your password, you must reset the configuration values stored in CMOS to defaults. Resetting CMOS requires opening up the system unit, so contact your dealer for assistance.

REMOVING A PASSWORD

If you enter Setup using the user password, you cannot modify or remove the supervisor password.

To remove a password, select the desired password to remove and press ← or →.

3.6.2 Diskette Drive Control

This parameter allows you to enable or disable the read/write functions of the floppy drive. The following table summarizes the available options.

Table 3-2 Diskette Drive Control Settings

Setting	Description
Normal (default)	Floppy drive functions normally
Write-Protect	Disables any floppy drive write function; protects all sectors only under DOS mode.

Disabled	Disables the floppy drive

3.6.3 Hard Disk Drive Control

This parameter allows you to enable or disable the read/write functions of the hard disk. The following table summarizes the available options.

Table 3-3 Hard Disk Drive Control Settings

Setting	Description
Normal (default)	Hard disk functions normally
Write-Protect	Disables any hard disk write function; protects all sectors only under DOS mode.
Disabled	Disables the hard disk

3.6.4 Start Up Sequences

This parameter determines which drive the system boots from when you turn on the system. The following table lists the five possible settings.

Table 3-4 Start Up Sequences Settings

Setting	Description
A: then C: (default)	System boots from floppy drive A. If the diskette is a non-system disk, the system boots from hard disk C.
C: then A:	System boots from hard disk C. If the hard disk is a non-system disk, the system boots from floppy drive A.
A: only	System boots from floppy drive A. If the floppy drive is a non-system disk, an error message appears.
C: only	System boots from hard disk C. If the hard disk is a non-system disk, an error message appears.
CD-ROM then C: then A:	System boots from a CD-ROM disc if one is installed in the CD-ROM drive. If no disc is present, the system boots from the hard disk C. If the hard disk is a non-system disk, then the system boots from floppy drive A.

3.6.5 Flash New BIOS

Contact your authorized dealer if you need to upgrade your BIOS.

INTRODUCTION ON FLASH BIOS AND BOOT BLOCK

The boot block is used to program and recover the system BIOS when the BIOS is destroyed and cannot perform normal boot. It also programs the new BIOS into the flash ROM if the item Flash New BIOS is set to [**Enabled**].

OPERATING INSTRUCTIONS FOR FLASHING IN A BIOS

There are two ways to flash in a new BIOS:

1. ***Hardware Jumper*** A hardware jumper is provided for the BIOS to distinguished from booting from the boot block or doing normal booting (see V1 GPIO pin 0).

   When the jumper is set, the boot ROM will first do POST (only to initialize the necessary components in the system), then read the BIOS binary file from the floppy disk drive (FDD) to the memory buffer. The file is (and should be) the first file in a DOS-formatted 1.44MB diskette. If two FDDs are connected to the system, the first one is used.

   After the system finishes reading the file from the FDD, the boot ROM will program the whole flash ROM except the boot block area. If the flash is successful, the FDD motor powers off and the system issues beeps to indicate that the programming has been completed. The user then powers off the system to take away the jumper then power up the system to boot from the new BIOS.

   If errors occur during the boot ROM process, the system issues a beep sequence (see table).

   Table 3-5 Error Beep Sequences During the Boot ROM Process

Description	Error Code	Beeps
First file size mismatch	0F1h	1 long beep, 1 short beep
File read error	0F2h	1 long beep, 2 short beeps
Flash ROM erase error	0E1h	2 long beeps, 1 short beep
Flash ROM programming error	0E2h	2 long beeps, 2 short beeps
No FDD	0D1h	2 short beeps

   When successful, the system gives off the following beep sequence — 2 long, 1 short, 1 long.

2. ***CMOS Setup*** An item (Flash New BIOS) allows you to flash in a new BIOS.

   When this item is set to **[Enabled]**, the user needs to issue a *hardware reset* by pressing the reset button (near the module bay near the rear of the system) or remove all power to flash the new BIOS. The boot ROM will do POST to initialize the necessary components, check the FDD and read in the new BIOS binary file (the same as method 1 except that when a FDD or BIOS binary file read error occurs, the boot ROM will go to POST normal boot.

   After the successful beep sequence sounds, the user has to set the Flash New BIOS item back to **[Disabled]** after programming the ROM and restarting the system.

3.7 Reset to Default Settings

Selecting this option allows you to load all the default settings. These settings are the values initially stored in CMOS RAM intended to provide high performance. If in the future you change these settings, you can load the default settings again by selecting this option.

When you select this option, the following prompt appears:

```
        Reset to Default Settings
             Are you sure?



         [Yes]        [No]
```

Select **`[Yes]`** to load the default settings or **`[No]`** to abort the operation.

Disassembly and Unit Replacement

This chapter contains step-by-step procedures on how to disassemble the notebook computer for maintenance and troubleshooting.

To disassemble the computer, you need the following tools:

- Wrist grounding strap and conductive mat for preventing electrostatic discharge
- Flat-bladed screwdriver
- Phillips screwdriver
- Hexagonal screwdriver
- Tweezers
- Plastic stick

The screws for the different components vary in size. During the disassembly process, group the screws with the corresponding components to avoid mismatch when putting back the components.

4.1 General Information

4.1.1 Before You Begin

Before proceeding with the disassembly procedure, make sure that you do the following:

1. Turn off the power to the system and all peripherals.

2. Unplug the AC adapter and all power and signal cables from the system.

3. Remove the battery pack from the notebook by (a) pressing the battery compartment cover release button, and (b) sliding out the cover. Then (c) pull out the battery pack.

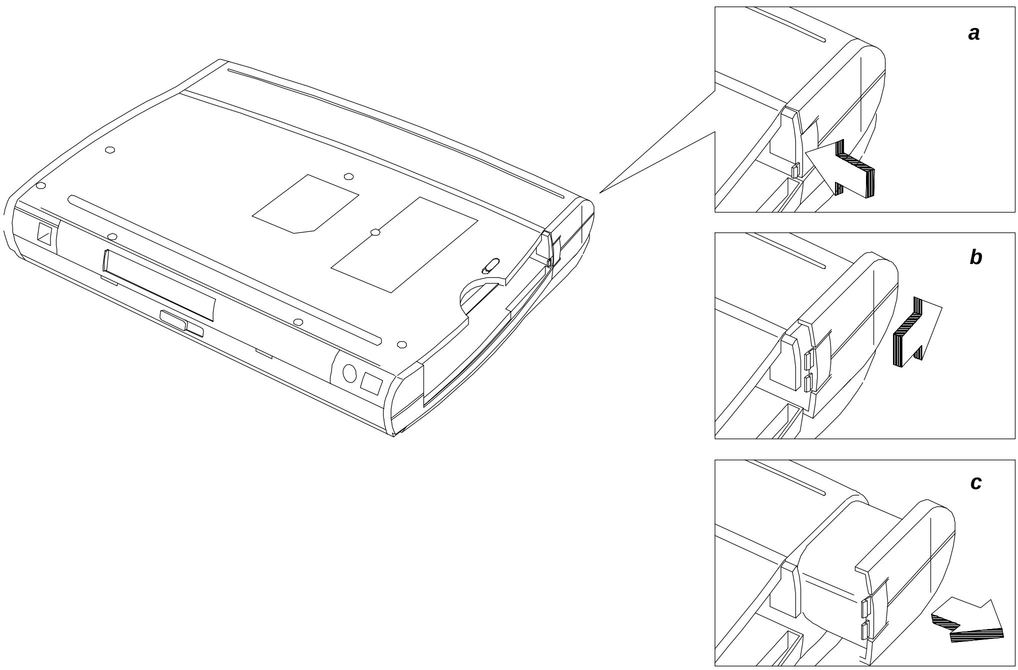


Figure 4-1 Removing the Battery Pack

Removing all power sources from the system prevents accidental short circuit during the disassembly process.

4.1.2 Connector Types

There are two kinds of connectors on the main board:

- Connectors with no locks

  Unplug the cable by simply pulling out the cable from the connector.

- Connectors with locks

  You can use a plastic stick to lock and unlock connectors with locks.

The cables used here are special FPC (flexible printed-circuit) cables, which are more delicate than normal plastic-enclosed cables. Therefore, to prevent damage, make sure that you unlock the connectors before pulling out the cables. Do not force cables out of the connectors.

<u>CONNECTORS WITH LOCKS</u>

- Unplugging the Cable

  To unplug the cable, first unlock the connector by pulling up the two clasps on both sides of the connector with a plastic stick. Then carefully pull out the cable from the connector.

- Plugging the Cable

  To plug the cable back, first make sure that the connector is unlocked, then plug the cable into the connector. With a plastic stick, press the two clasps on both sides of the connector to secure the cables in place.

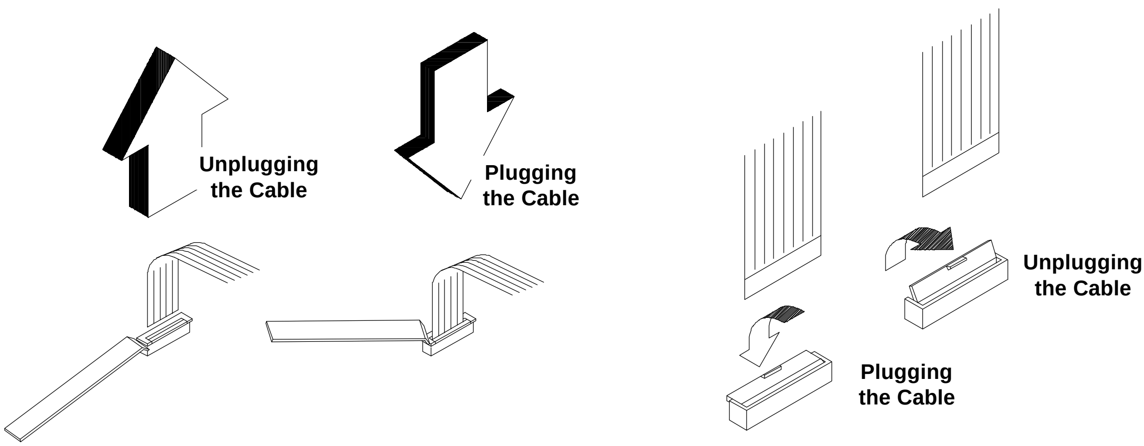


Figure 4-2 Using Plastic Stick on Connector With Locks

Connectors mentioned in the following procedures are assumed to be no-lock connectors unless specified otherwise.

4.1.3 Disassembly Sequence

The disassembly procedure described in this manual is divided into four major sections:

- Section 4.2: Removing the module
- Section 4.3: Removing the keyboard
- Section 4.4: Removing the hard disk drive
- Section 4.5: Disassembling the inside assembly frame
- Section 4.6: Disassembling the display

The following table lists the components that need to be removed during servicing. For example, if you want to remove the motherboard, you must first remove the keyboard, then disassemble the inside assembly frame in that order.

Table 4-1 Guide to Disassembly Sequence

Service Item	Prerequisite
Install CPU	Remove the keyboard.
Remove the keyboard	Remove two speaker covers on both sides and one center hinge cover.
Remove or replace the hard disk drive	Remove the lower unit of lower case
Install additional memory SIMM socket 1 SIMM socket 2	 Remove the lower unit of lower case Remove the SIMM door.
Remove the touchpad	1. Remove the keyboard. 2. Remove the LCD display module. 3. Remove the upper unit of lower case.
Replace the LCD	Remove the LCD display module.
Remove the motherboard for service or replacement	1. Remove the keyboard. 2. Remove the LCD display module. 3. Remove the lower unit of lower case.

The following diagram details the disassembly flow.

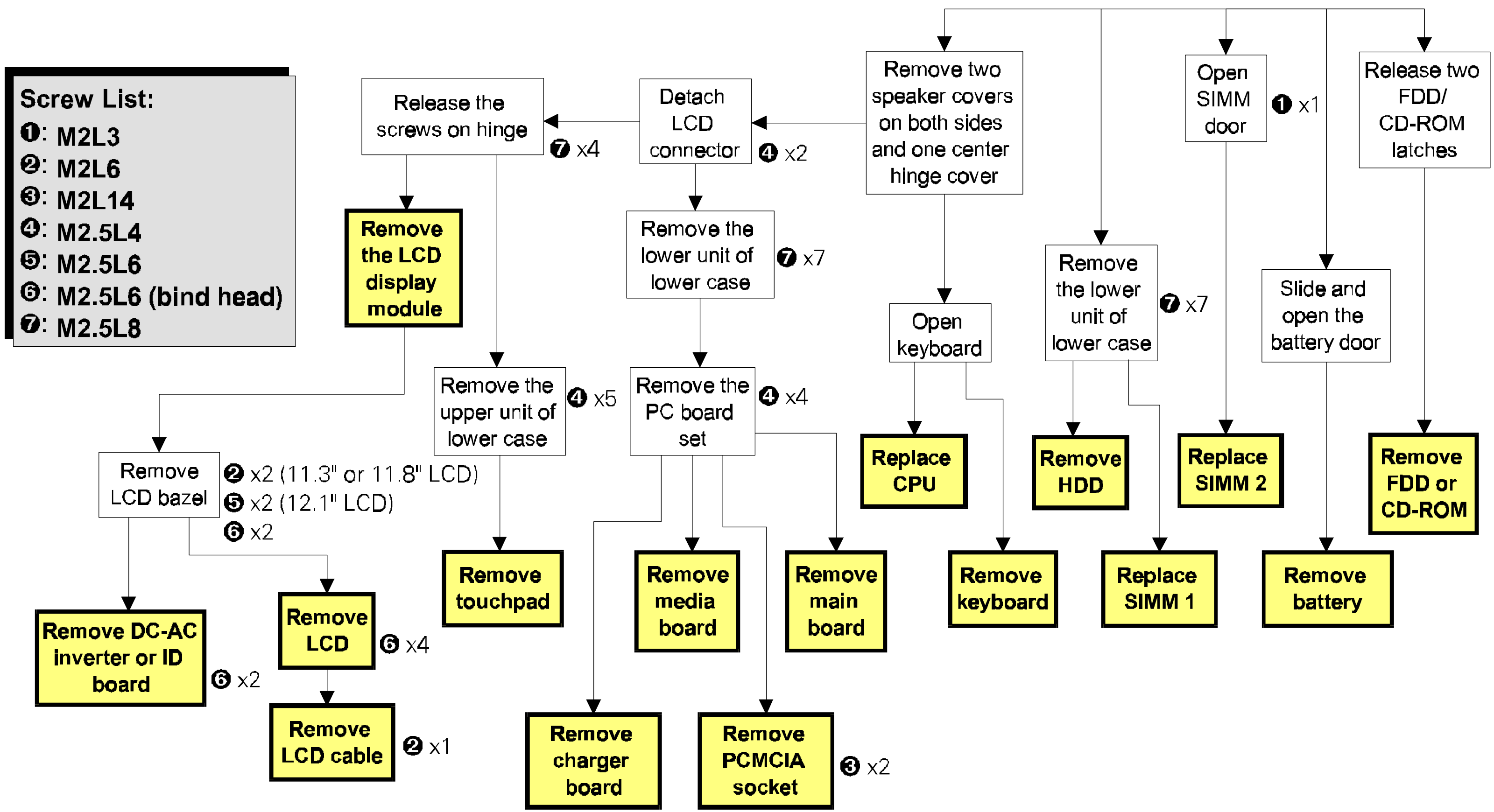


Figure 4-3 Disassembly Flow

4.2 Removing the Module

If you are going to disassemble the unit, it is advisable to remove the module first before proceeding. Follow these steps to remove the module:

1. Slide out and hold the module release button.

2. Press the module release latch and slide out the module.

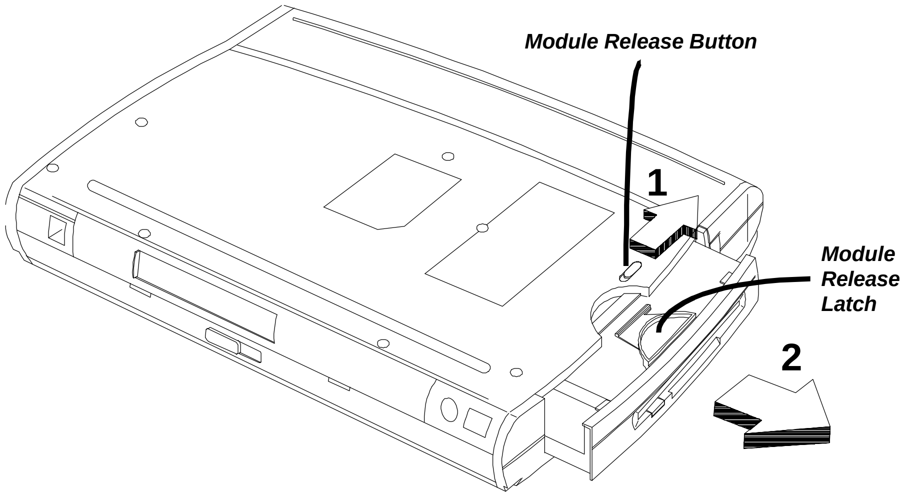


Figure 4-4 Removing the Module

4.3 Removing the Keyboard

Follow these steps to remove the keyboard:

1. Slide out the two display hinge covers on both sides of the notebook.

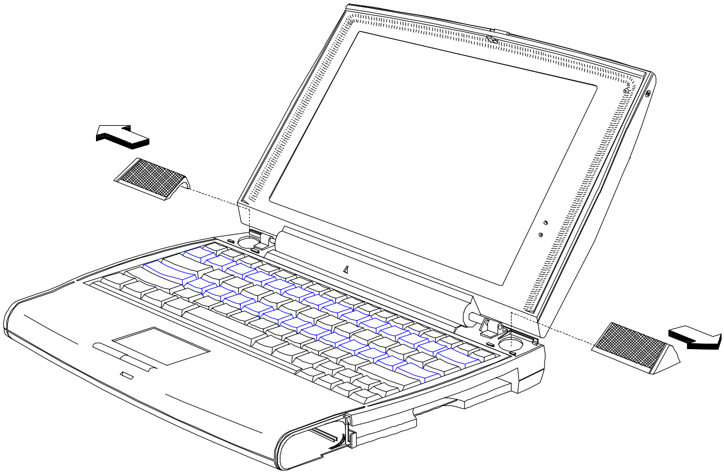


Figure 4-5 Removing the Display Hinge Covers

2. Pull out (first from the edges) and remove the center hinge cover.

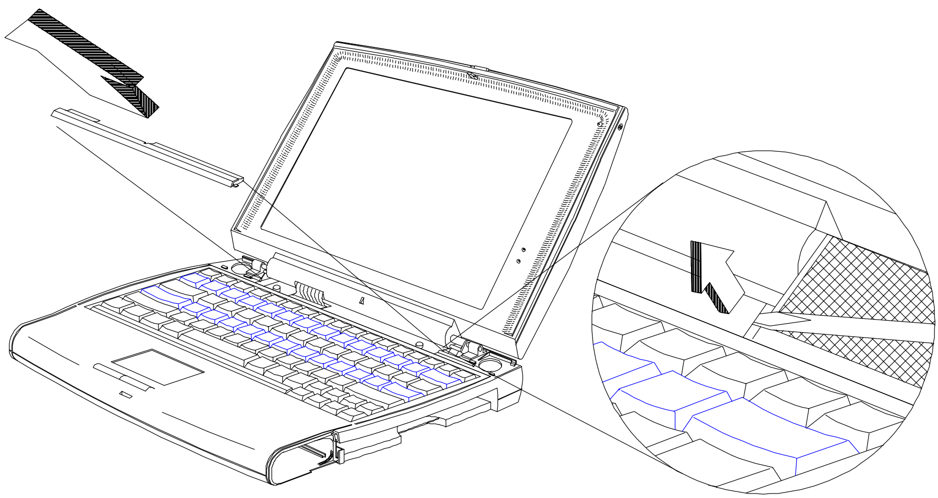


Figure 4-6 Removing the Center Hinge Cover

3. Lifting out the keyboard takes three steps — (a) lifting up the keyboard, (b) rotating the keyboard to one side, and (c) pulling out the keyboard in the opposite direction.

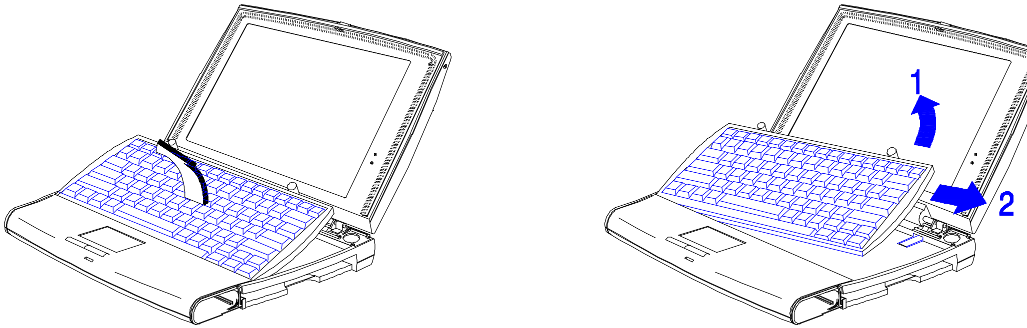


Figure 4-7 Lifting Out the Keyboard

4. Flip the keyboard over and unplug the keyboard connectors (CN4, CN2) to remove the keyboard.

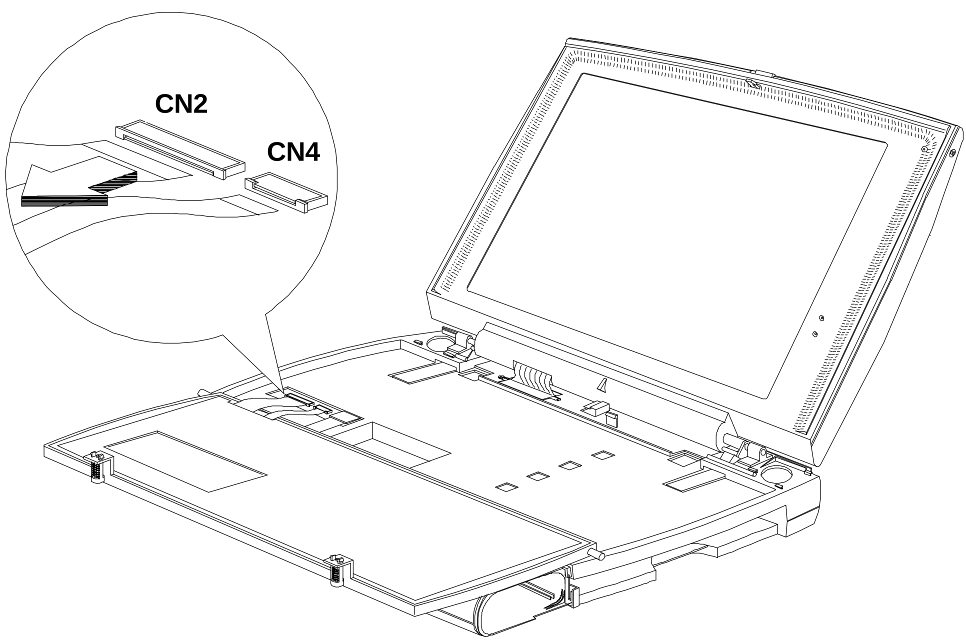


Figure 4-8 Unplugging the Keyboard Connectors and Removing the Keyboard

4.3 Removing or Replacing the CPU

Follow these steps to remove the CPU module.

1. The CPU module is locked in place by a metal lock which needs to be pulled back and removed before the CPU module can be removed.

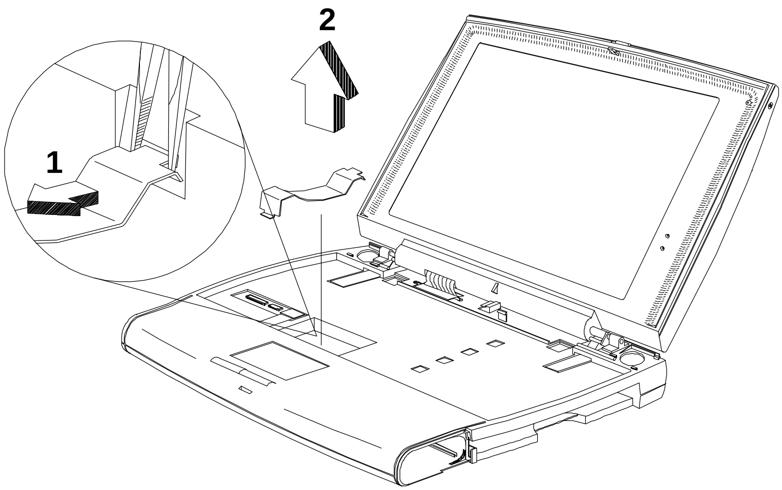


Figure 4-9 Removing the CPU Module Lock

2. Pull up the module using the module handle. (CN8, CN12)



When inserting a CPU module, take note of the female and male connectors on the CPU module. These should match the corresponding male and female connectors on the main board.

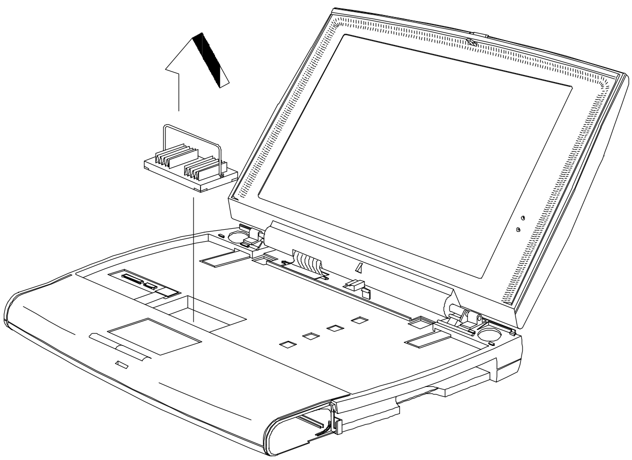


Figure 4-10 Removing the CPU Module

4.4 Removing the Display

Follow these steps to remove the display module.

1. Remove the two screws that secure the display cable to the motherboard. Then unplug the display cable (CN6).

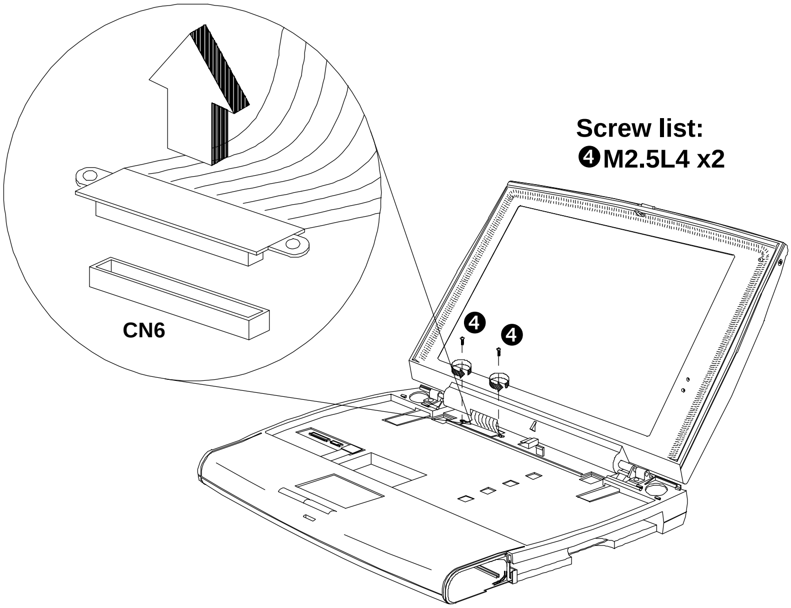


Figure 4-11 Unplugging the Display Cable

2. Remove the four display hinge screws. Detach the display from the main unit and set aside.

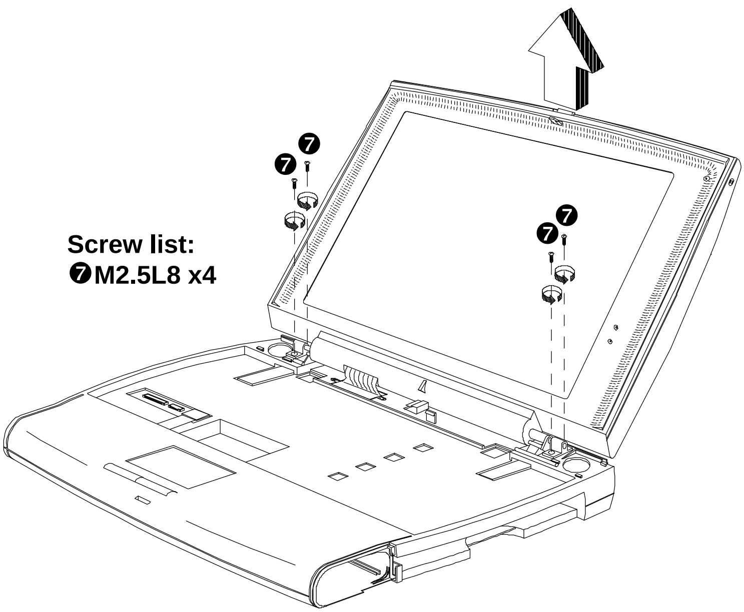


Figure 4-12 Removing the Display Hinge Screws and Removing the Display

4.5 Disassembling the Housing

This section discusses how to disassemble the housing, and during its course, includes removing and replacing of certain major components like the hard disk drive, memory and the main board.

4.5.1 Detaching the Lower Housing from the Inside Assembly

To detach the lower housing from the inside assembly, turn the unit over and remove seven (7) base screws. Then snap out the lower part of the housing.

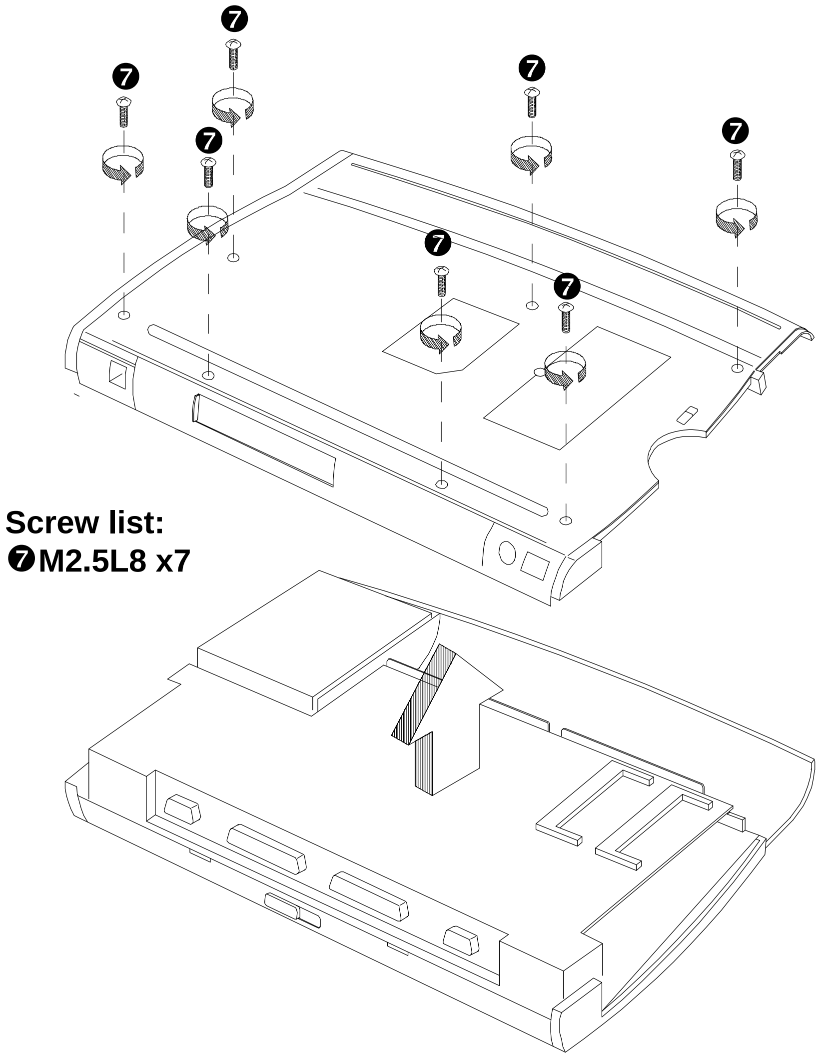


Figure 4-13 Removing the Hard Disk Drive Bay Cover

Detaching the lower housing from the inside frame assembly allows you to remove/install the hard disk drive, as well as remove/install memory modules.

4.5.2 Replacing the Hard Disk Drive

Follow these steps:

1. Remove two screws that secure the hard disk drive to the inside frame assembly.

2. Turn the hard disk drive over and pull out the hard disk drive cable from its connector.

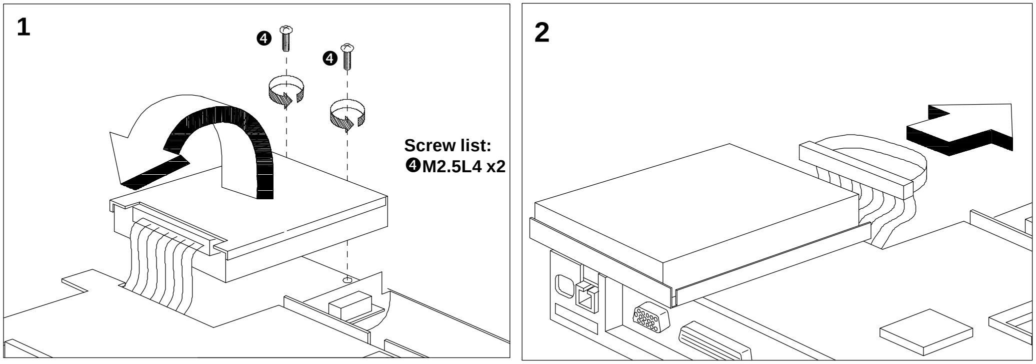


Figure 4-14 Removing the Hard Disk Drive Bay Cover

If you want to install a new hard disk drive, reverse the steps described above.

4.5.3 Replacing Memory

Both memory slots (SIMM1 and SIMM2) are accessible after detaching the lower housing from the inside frame assembly. You or the user can also upgrade memory (via one of the two available memory slots, SIMM1) without disassembling the housing — accessed by opening the memory upgrade door at the base of the unit.

Installing Memory Module(s)

Follow these steps to install memory module(s):

1. Remove the memory module(s) from its shipping container.

2. Align the connector edge of the memory module with the key in the connector. Insert the edge of the memory module board into the connector. Use a rocking motion to fully insert the module. Push downward on each side of the memory module until it snaps in place.

   To remove the memory module, release the slot locks found on both ends of the memory slot to release the DIMM. Then pull out the memory module.

4.5.4 Detaching the Upper Housing from the Inside Assembly

Follow these steps:

1. Remove three screws in the battery bay.

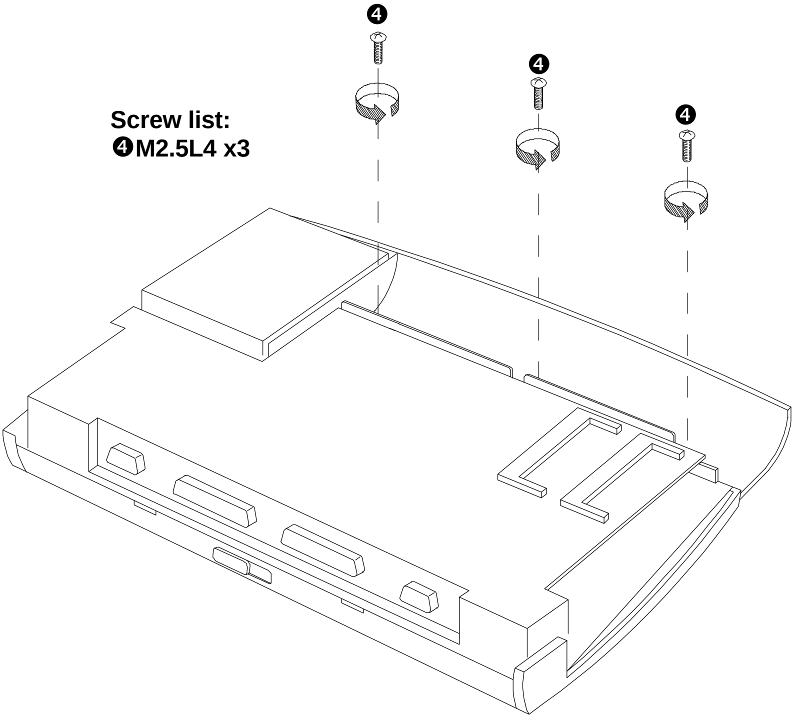


Figure 4-17 Removing the Battery Bay Screws

2. Turn the unit back over and remove two screws close to the back part of the unit. Then snap out the upper part of the housing — (1) first from the rear of the unit, then (2) the front end of the unit.

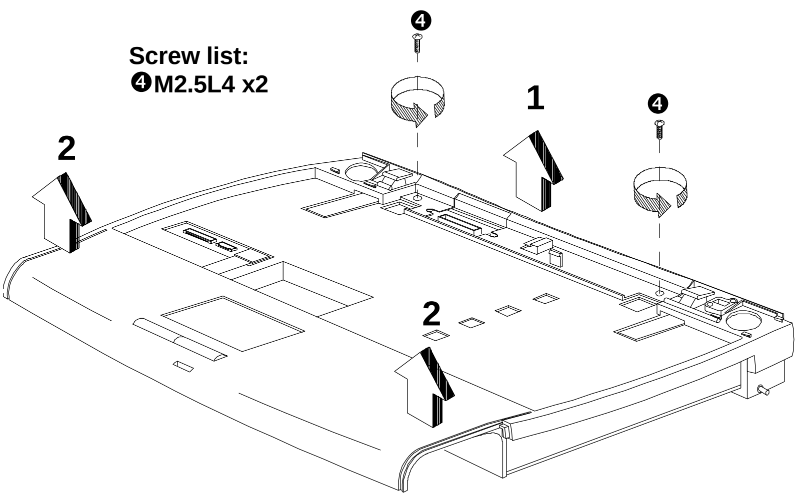


Figure 4-18 Detaching the Upper Housing from the Inside Frame Assembly

4.5.5 Removing the Touchpad

Follow these steps to remove the touchpad:

1. Unplug the touchpad connector (CN5).

2. Pull up and remove the touchpad.

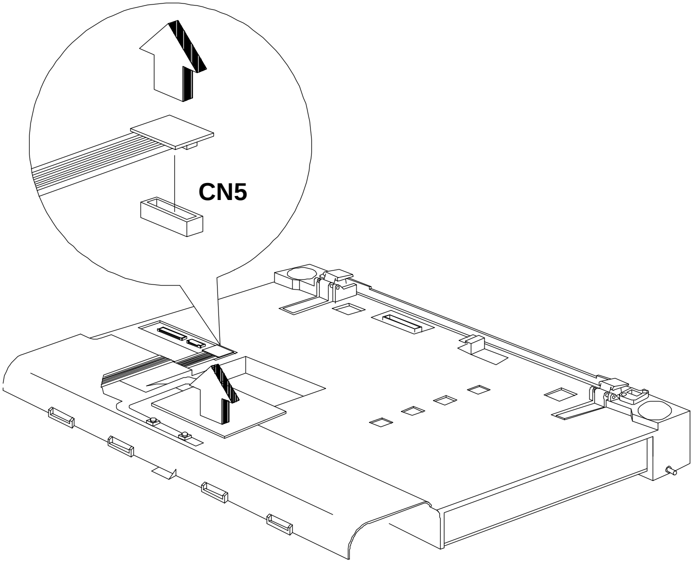


Figure 4-19 Removing the Touchpad

4.5.6 Removing the Main Board

Follow these steps to remove the main board from the inside assembly.

1. Unplug the speaker connectors (CN17 and CN23), and the battery pack connector (CN21).

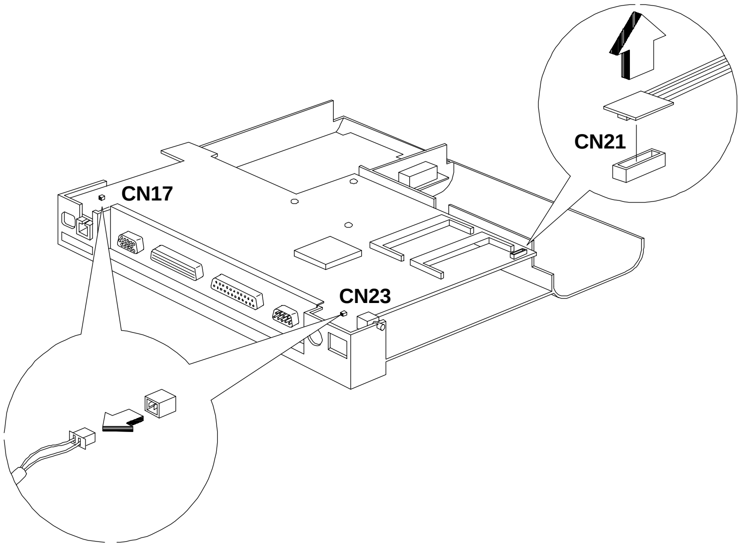


Figure 4-20 Unplugging the Speaker Connectors and Battery Pack Connector

2. Remove three screws (and gaskets) to remove the main board from the inside assembly.

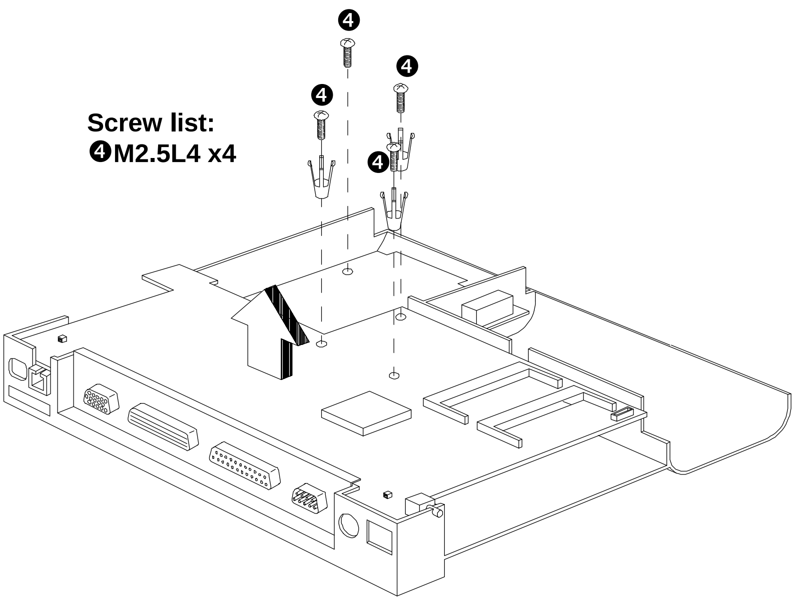


Figure 4-21 Removing the Main Board

3. Remove the charger board (CN19 and CN20) and the multimedia board (CN10 and CN7) from the main board.

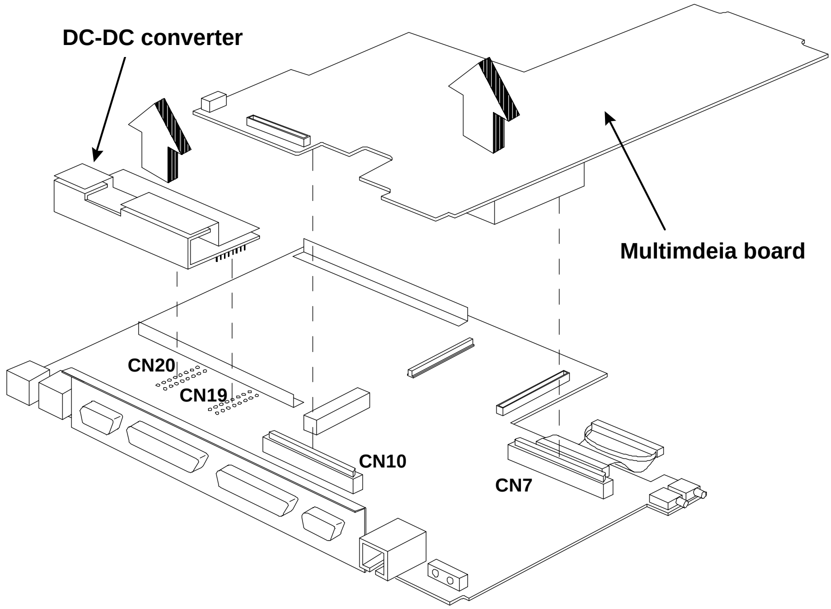


Figure 4-22 Removing the Charger Board and Multimedia Board

4. The PC card slot module is usually part of the main board spare part. This removal procedure is for reference only. To remove the PC card slot module, remove two screws.

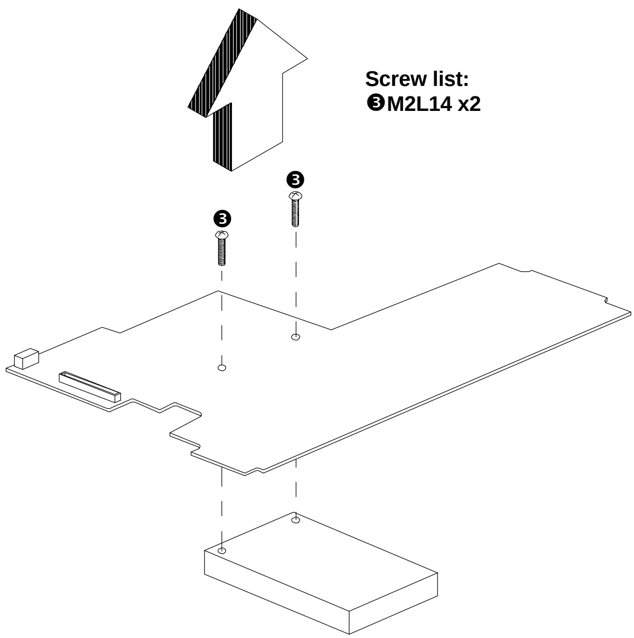


Figure 4-23 Removing the PC Card Slots

4.5 Disassembling the Display

Follow these steps to disassemble the display:

1. Remove the teardrop-shaped LCD bumpers at the top of the display and the long bumper on the LCD hinge.

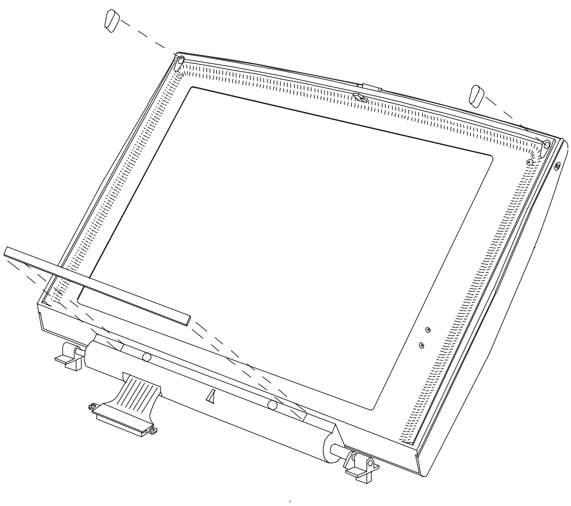
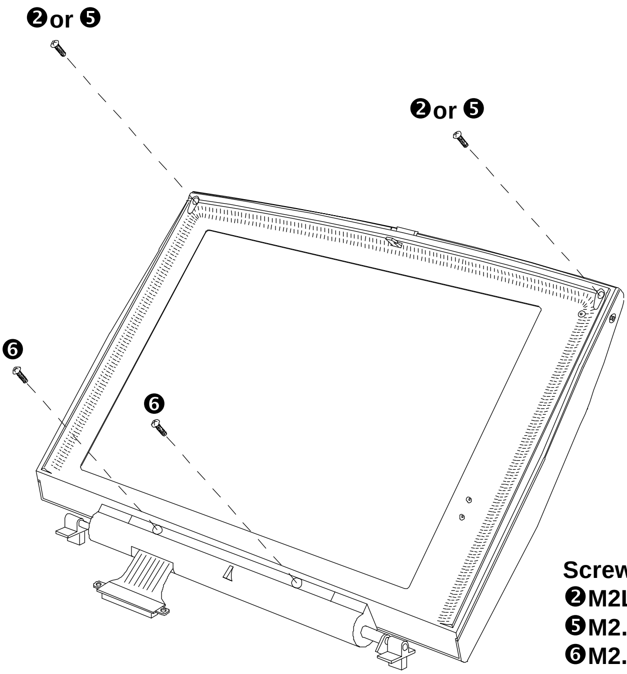


Figure 4-24 Removing the LCD Bumpers

2. Remove four screws on the display bezel.



Screw list:
❷M2L6 x2 (for 11.3” or 11.8” LCD)
❺M2.5L6 x2 (for 12.1” LCD)
❻M2.5L6(bind head) x2

Figure 4-25 Removing the Display Bezel Screws

3. Pull out and remove the display bezel by pulling on the inside of the bezel sides.

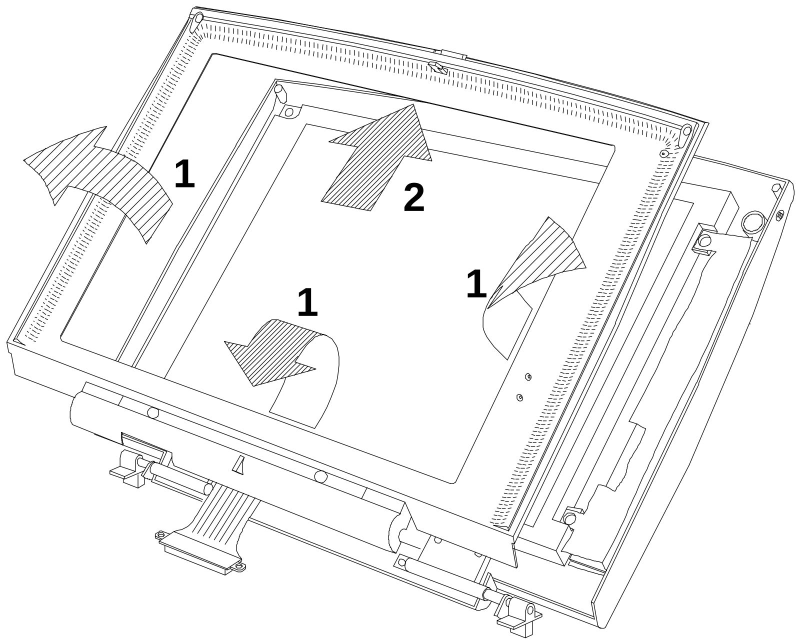


Figure 4-26 Removing the Display Bezel

4. Remove the four display panel screws, and unplug the inverter and display panel connectors. Then tilt up and remove the display panel.

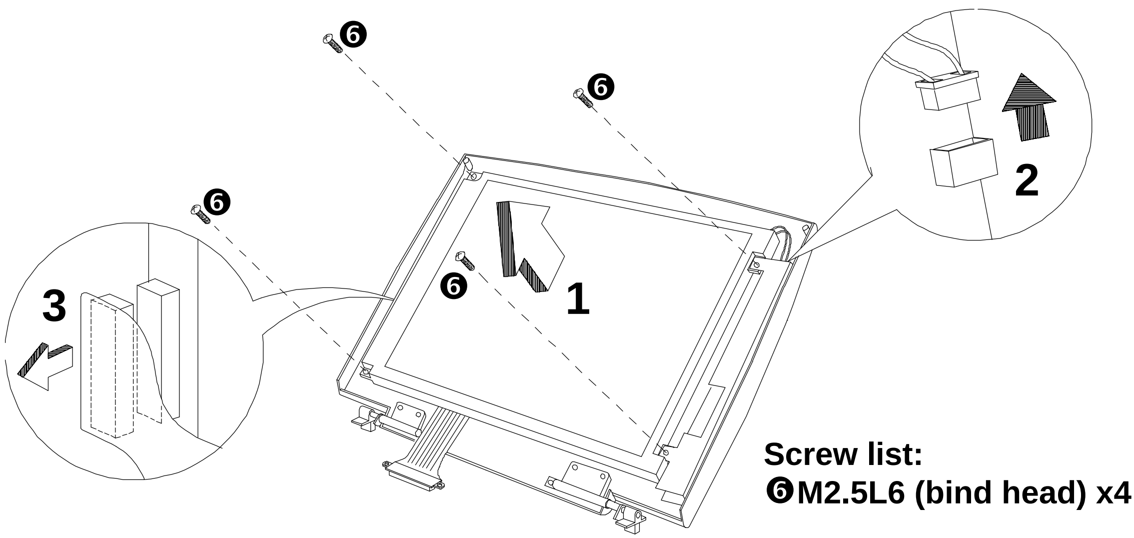


Figure 4-27 Removing the Display Panel Screws and the Display Connectors

5. Remove the two display assembly screws and unplug the display cable connector from the display cable assembly. Then remove the LCD inverter and ID boards.

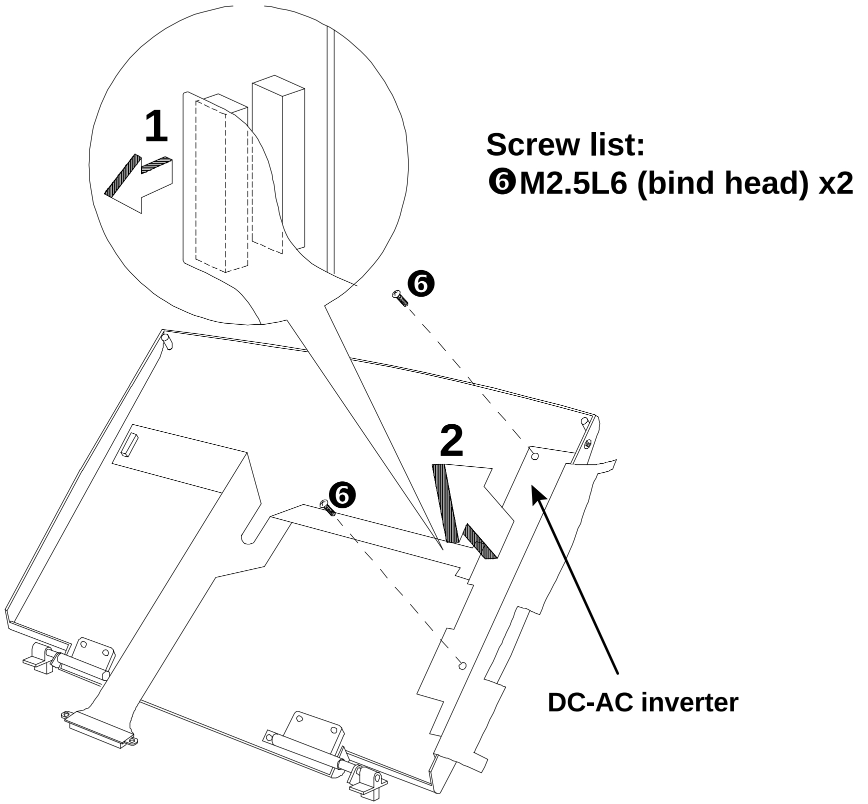


Figure 4-28   Removing the Display Cable Assembly

Model Number Definition

This appendix shows the model number definition of the notebook.

A.1 970C

970C-X Y Z

- Z → **Keyboard Language Version**
- Y → **Memory & CPU & LCD**
- X → **HDD & FDD & CD-ROM & Fax/Modem**

Keyboard Language Version

0: Swiss/US
1: US (110V)
2: US (220V)
3: US w/o power cord
4: US K/B w/o power cord (ACLA)
5: US (110V for AAB)
7: Spanish w/o power cord
8: Turkish
A: Arabic
C: Chinese
D: Danish
F: French
G: German
H: Hebrew
I: Italian
J: Japanese
K: Korean
N: Norwegian
S: Spanish (220V)
T: Thailand
U: UK (250V)
W: Swedish/Finnish
X: Swiss/German
Y: Swiss/French
Z: w/o keyboard

Memory & CPU & LCD

0: 0MB + No CPU + 11.3" STN SVGA Hitachi 9930
1: 0MB + No CPU + 11.3" STN SVGA Sanyo FH53
6: 16MB + P54CSLM-120 + 11.3" STN SVGA Hitachi 9930
7: 16MB + P54CSLM-120 + 11.3" STN SVGA Sanyo FH53
8: 16MB + P54CSLM-133 + 11.3" STN SVGA Hitachi 9930
9: 16MB + P54CSLM-133 + 11.3" STN SVGA Sanyo FH53
A: 16MB + P54CSLM-150 + 11.3" STN SVGA Hitachi 9930
M: 16MB + P54CSLM-133 + 11.3" STN SVGA Hitachi 9930 + Bulk Pack
N: 16MB + No CPU + 11.3" STN SVGA Sanyo FH53 + Bulk Pack
V: 16MB + P54CSLM-133 + 11.3" STN SVGA Hitachi 9930 + Generic Panel/076
X: 16MB + P54CSLM-133 + 11.3" STN SVGA Hitachi 9930 + Generic Panel/050

HDD & FDD & CD-ROM & Fax/Modem

0: No HDD + FDD + No CD-ROM + No Fax/Modem
1: No HDD + FDD + No CD-ROM + Fax/Modem
2: 1.0GB HDD + FDD + CD-ROM + No Fax/Modem
3: 1.0GB HDD + FDD + CD-ROM + Fax/Modem
4: 1.2GB HDD + FDD + CD-ROM + No Fax/Modem
5: 1.2GB HDD + FDD + CD-ROM + Fax/Modem
8: 1.35GB HDD + FDD + CD-ROM + No Fax/Modem
9: 1.35GB HDD + FDD + CD-ROM + Fax/Modem
A: 1.35GB HDD + No FDD + CD-ROM + Fax/Modem
B: 1.35GB HDD + FDD + No CD-ROM + Fax/Modem
G: 2.0GB HDD + FDD + CD-ROM + No Fax/Modem
H: 2.0GB HDD + FDD + CD-ROM + Fax/Modem

A.2 970CX

970CX-X Y Z

Keyboard Language Version (Z)

0:	Swiss/US	H:	Hebrew
1:	US (110V)	I:	Italian
2:	US (220V)	J:	Japanese
3:	US w/o power cord	K:	Korean
4:	US K/B w/o power cord (ACLA)	N:	Norwegian
5:	US (110V for AAB)	S:	Spanish (220V)
7:	Spanish w/o power cord	T:	Thailand
8:	Turkish	U:	UK (250V)
A:	Arabic	W:	Swedish/Finnish
C:	Chinese	X:	Swiss/German
D:	Danish	Y:	Swiss/French
F:	French	Z:	w/o keyboard
G:	German		

Memory & CPU & LCD (Y)

0: 0MB + No CPU + 11.8" TFT SVGA Hitachi TX30D
4: 16MB + P54CSLM-133 + 11.8" TFT SVGA Hitachi TX30D
5: 16MB + P54CSLM-150 + 11.8" TFT SVGA Hitachi TX30D
7: 16MB + P54CSLM-133 + 12.1" TFT SVGA IBM ITSV50D
8: 16MB + P54CSLM-150 + 12.1" TFT SVGA IBM ITSV50D
M: 16MB + P54CSLM-133 + 11.8" TFT SVGA Hitachi TX30D + Bulk Pack
N: 16MB + P54CSLM-133 + 12.1" TFT SVGA IBM ITSV50D + Bulk Pack
R: 16MB + P54CSLM-133 + 11.8" TFT SVGA Hitachi TX30D + Generic Panel

HDD & FDD & CD-ROM & Fax/Modem (X)

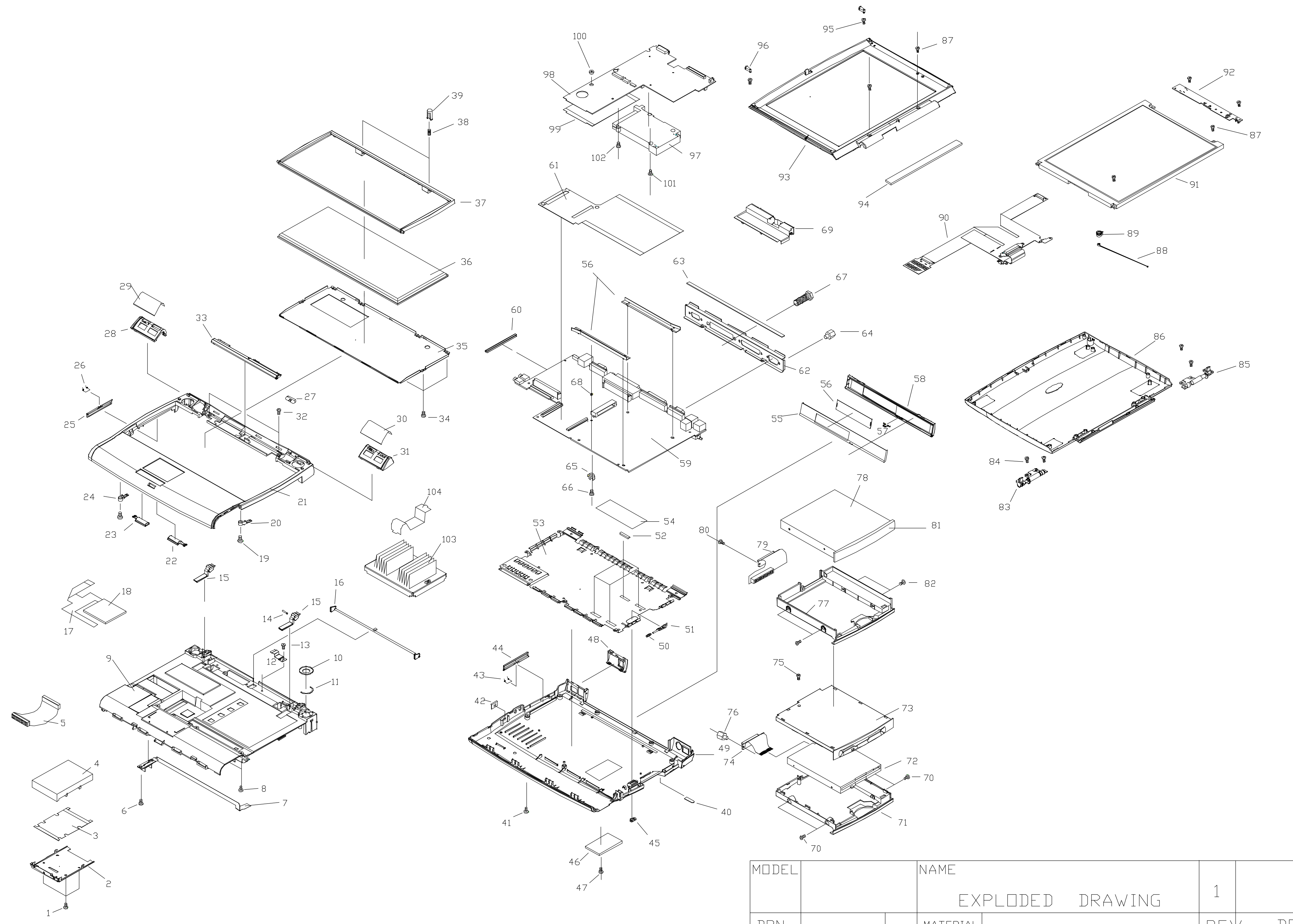
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3: 1.0GB HDD + FDD + CD-ROM + Fax/Modem
4: 1.2GB HDD + FDD + CD-ROM + No Fax/Modem
5: 1.2GB HDD + FDD + CD-ROM + Fax/Modem
8: 1.35GB HDD + FDD + CD-ROM + No Fax/Modem
9: 1.35GB HDD + FDD + CD-ROM + Fax/Modem
A: 1.35GB HDD + No FDD + CD-ROM + Fax/Modem
B: 1.35GB HDD + FDD + No CD-ROM + Fax/Modem
G: 2.0GB HDD + FDD + CD-ROM + No Fax/Modem
H: 2.0GB HDD + FDD + CD-ROM + Fax/Modem

Item	Part No.	Description
1	86.5A224.4R0	SCRW MACH FLAT M3*4L ZN
2	34.46803.001	COVER HDD AL 970
3	42.46842.001	MYLAR HDD PC 970
4	56.02941.001	HDD 2160MB IBM/DCRA-22160 ATA
5	50.42003.002	CABLE ASSY FPC 44P 43MM
	60.46803.023	ASSY CHASSIS MAIN 970
6	86.1A553.4R0	SCRW MACH PAN NYLOK M2.5*4L NI
7	50.46807.001	CABLE ASSY 8P #24 BTY 970
8	86.1A553.4R0	SCRW MACH PAN NYLOK M2.5*4L NI
9	34.46810.001	CHASSIS MAIN MG 970
10	23.40015.031	SPK T023S03T0013 D23 W/CAB65MM
11	38.46802.001	TAPE ADHESIVE FOR SPEAKER 970
12	34.46839.001	SPRING COVER SWITCH SUS301 970
13	86.1A553.4R0	SCRW MACH PAN NYLOK M2.5*4L NI
14	34.46814.001	LIFTER SHAFT STEEL 970
15	34.46806.002	LIFTER KEYBOARD AL 970
16	34.46801.001	LINK LIFT DISABLE STEEL 970
17	50.46808.001	CABLE ASSY FPC TOUCH PAD 970
18	56.17468.001	TOUCHPAD SYNAPTIC/TM1002SC 970
	60.46807.001	ASSY CASE UPPER 050 970
19	86.6A522.4R0	SCREW MECH RWH M2*4L NI
20	42.46803.001	RAIL R KEYBD NYLON66 050 970
21	39.46802.001	CASE UPPER PC+10GF 050 970
22	42.46847.001	KNOB(R) TOUCH ABS 050 970
23	42.46812.001	KNOB(L) TOUCH ABS 050 970
24	42.46802.001	RAIL L KEYBD NYLON66 050 970
25	42.46806.001	DOOR CARDBUS PC+10%GF 050 970
26	34.46811.001	SPRING DOOR CARDBUS SUS301 970
27	42.46811.001	KNOB TILT DISABLE ABS 050 970

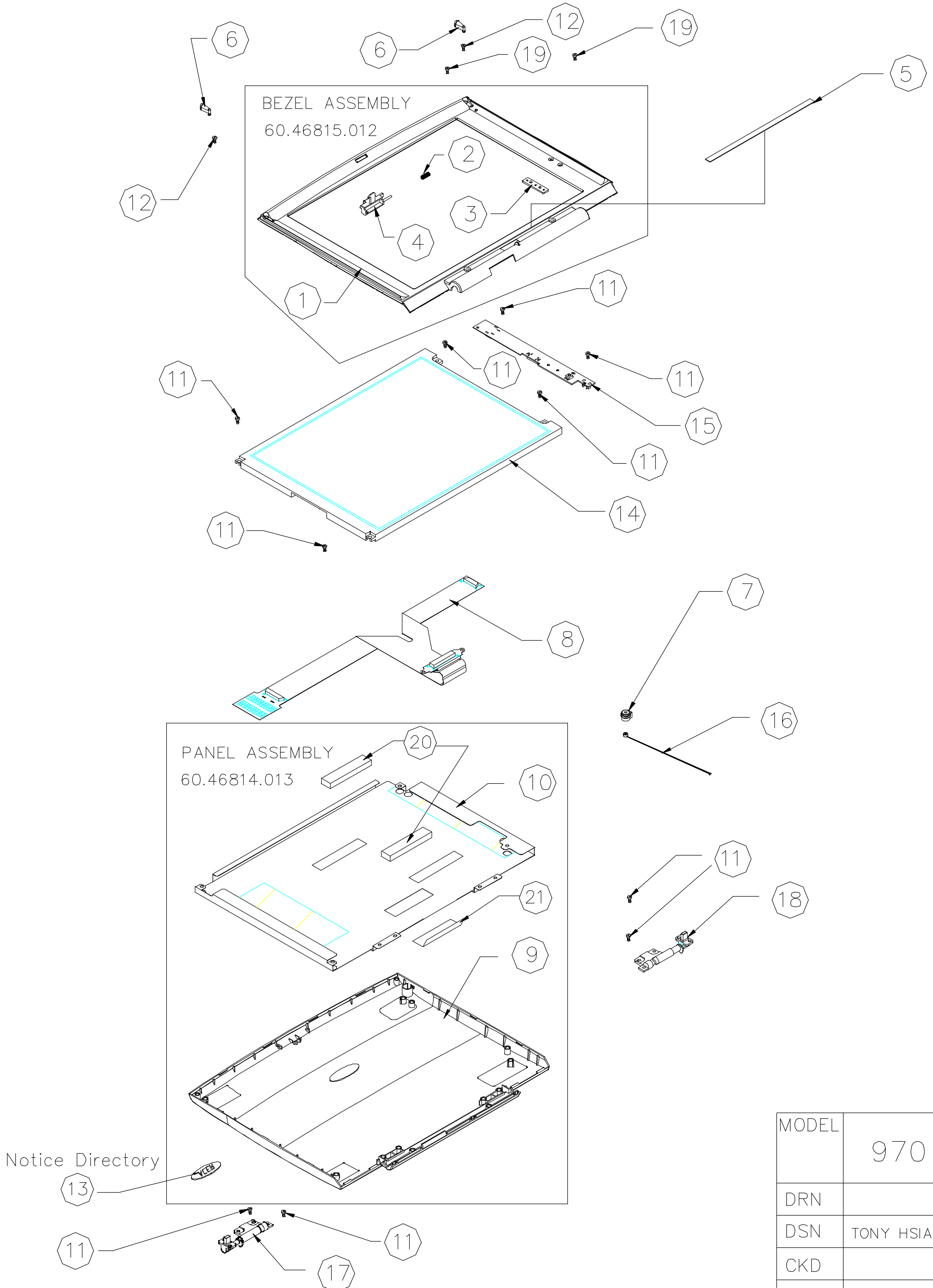
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29	31.46815.001	SPEAKER NET(L) SPTH 000 970
30	31.46814.001	SPEAKER NET(R) SPTH 000 970
31	42.46824.001	COVER R HINGE PC+10%GF 050 970
32	86.6A522.4R0	SCREW MECH RWH M2*4L NI
33	42.46822.001	COVER MIDDLE PC+10%GF 050 970
	90.46807.001	KB-84 KEY KAS1901-0111R US
34	86.1A522.3R0	SCRW MACH PAN M2*3L NI
35	34.46805.001	FRAME KEYBOARD SECC 970
36	90.46807.001	KB-84 KEY KAS1901-0111R US
37	42.46816.001	COVER KB PC+10%GF 050 970
38	34.46812.001	SPRING FIX KEYBOARD SUS301
39	42.46817.001	HOLDER SPRING ABS 050 970
	60.46808.002	ASSY CASE LOWER 050 970
40	47.46812.001	RUBBER FOOT 000 970
41	86.1A553.8R0	SCRW MACH PAN NYLOK M2.5*8L NI
42	31.46812.001	PLT KEY-LOCK REING SUS301 970
43	34.46811.001	SPRING DOOR CARDBUS SUS301 970
44	42.46806.001	DOOR CARDBUS PC+10%GF 050 970
45	42.46813.001	KNOB LOCK MDUL ABS 050 970
46	34.46850.002	DOOR DIMM AL 970
47	86.1A522.2R0	SCRW MACHINE PAN M2*2 NI
48	42.46853.001	COVER SIR BACK(NO RJ11) PC 970
49	39.46801.001	CASE LOWER PC+10GF 050 970
50	34.46813.001	SPRING HOOK MODULE SUS301 970
51	42.46814.001	HOOK LOCK MDUL NYLON 050 970
52	42.429A8.001	GASKET EMI 71TS4-1 900
53	31.46803.001	PLATE SHD L CASE EMI SPTH 970
54	40.46806.001	MYLAR LOWER CASE PC 970
55	42.46818.001	DOOR SLIDE PC+10%GF 050

Item	Part No.	Description
		970
56	42.46819.001	DOOR I/O INS PC+ABS 050 970
57	33.46802.001	SUPPORTER I/O DOOR SUS 301 970
58	42.46820.001	DOOR I/O PC+ABS 050 970
59	55.46801.001	MAIN BD W/O CPU 0MB 970
60	42.429A8.001	GASKET EMI 71TS4-1 900
61	42.46842.011	MYLAR MAIN BOARD PC 970
62	33.46801.001	BRACKET I/O AL 970
63	42.429A8.001	GASKET EMI 71TS4-1 900
64	34.00015.071	SCRW HEX I#4-40/O#4-40 L5.5 NI
65	31.46816.001	PLATE CPU EMI GND STEEL 970
66	86.1A522.6R0	SCRW MACH PAN M2*6L NI
67	34.46840.001	SCRW SOCKET STEEL M5*14AMP 970
68	87.11242.200	NUT HEX M2*0.4 D NI
69	19.20084.011	CONVERTER DC-DC T62.036.C 970
70	86.1A522.3R0	SCRW MACH PAN M2*3L NI
71	60.46822.002	ASSY FDD L-CASE 050 970
72	56.01051.071	FDD 1.44 3.5" D353F2 000(3MODE
73	42.46846.002	CASE UP FDD PC+GF 050 970
74	50.46802.001	CABLE ASSY FDD 52P 970
75	86.1A522.6R0	SCRW MACH PAN M2*6L NI
76	34.42801.001	STANDOFF HEX M2.5*0.45 9MM
77	42.46809.001	CHASSIS CD-ROM PC+10GF 050 970
78	56.10071.081	CD DRV TOSH/XM1402B 6X AT
79	50.46804.001	ASSY CD-ROM CABLE 52P 970
80	86.1A553.4R0	SCRW MACH PAN NYLOK M2.5*4L NI
81	60.46821.001	ASSY CD ROM BEZEL 050 970
82	86.1A522.3R0	SCRW MACH PAN M2*3L NI
83	34.46829.001	HINGE (L) AL 970
84	86.4A553.6R0	SCREW BIND MACH M2.5*6L NI
85	34.46830.001	HINGE (R) AL 970
86	60.46814.022	ASSY LCD PANEL(12.1")050 970
87	86.4A553.6R0	SCREW BIND MACH M2.5*6L NI

Item	Part No.	Description
88	23.42009.001	MICROPHONE 54DB KUC8723-030839
89	47.46803.001	CSN MICROPHONE SILICON 000 970
90	50.46801.001	CABLE ASSY 80P FPC 970
91	56.07468.001	IBM 12.1"TFT SVGA SV50D
92	19.21030.041	INVERTER T62.055.C 970
93	60.46815.031	ASSY LCD BZL(12.1")050 970
94	40.46805.001	PLATE LOGO(2) PC 050 97\0
95	86.4A553.6R0	SCREW BIND MACH M2.5*6L NI
96	47.46802.001	CUSHION BEZEL SILCON 000 970
97	21.H0007.001	CONN CARD PUSH C-11093 EJECT
98	55.46803.021	MEDIO BOARD W/O MODEM 970
99	40.46802.001	MYLAR MUTI-MIDI BD PC 970
100	33.46803.001	BRKET MEDIA BD FIX COPPER 9710
101	86.1A522.140	SCRW MACH PAN M2*14L NI
102	86.1A522.6R0	SCRW MACH PAN M2*6L NI
103	60.46802.011	ASSY HSINK CPU 970
104	31.46817.002	PLT SPRING CPU FIX SUS 970
	60.46814.011	ASSY LCD PANEL 11.3" 970
	60.46815.011	ASSY LCD BEZEL 11.3" 970
	56.07469.091	HITACHI 11.3"DSTN SVGA 9930
	50.46806.001	CABLE ASSY FPC (11.3"HIT) 970
	19.20086.001	INVERTER T62.039.C 970
	60.46814.001	ASSY LCD PANEL 11.8" 970
	60.46815.001	ASSY LCD BEZEL 11.8" 970
	56.07355.021	HITACHI 11.8" TFT SVGA TB0D01
	50.46801.001	CABLE ASSY (11.8"HIT) 970
	19.20086.001	INVERTER T62.039.C 970
	60.46814.021	ASSY LCD PANEL 12.1" 970
	60.46815.031	ASSY LCD BEZEL 12.1" 970
	56.07468.001	IBM 12.1"TFT SVGA SV50D
	50.46809.001	C.A.80P FPC(12.1"IBM) 970
	19.21030.041	INVERTER T62.055.C 970



MODEL		NAME EXPLODED DRAWING		1		
DRN		MATERIAL		REV	DESCRIPTION	SIGN DATE
DSN		FINISH			DIM IN mm	DO NOT SCALE DWG
CKD		Acer Incorporated			SHEET 1	OF
APPD				DRAWING NO.	91.46801.xxx	



91.46801.001/65.46806.001 LCD MODULE ASSEMBLY(SANYO 11.3")

No	Part No.	Description	Q'TY	Remark
01	41.46805.002	LCD BEZEL FOR HIT 11.3"	1	S.J.
02	34.47604.001	HOOK SPRING,EJ SPG	1	H.C.
03	42.46829.001	LED LENS,FOR POWER	1	S.J.
04	42.46828.001	LCD LATCH	1	S.J.
05	40.46805.001	ACER LOGO	1	S.Y.
06	47.46802.001	CUSHION BEZEL	2	P.M.
07	47.46803.001	CUSHION MICROPHONE	1	P.M.
08	50.46806.001	FPC LCD (HIT 11.3")	1	ADFLEX
09	41.46804.002	LCD PANEL FOR HIT 11.3"	1	S.J.
10	34.46831.002	EMI SHIELD FOR HIT 11.3"	1	S.Y.
11	86.4A453.6R0	SCREW PAN M2.5*L6 NYLON	10	CASHI
12	86.1A522.6R0	SCREW PAN MECH M2.0*L6	2	CASHI
13	31.46813.001	NAME PLATE, FOR ACER	1	OUDENSHA
14	56.07469.001	LCD SANYO 11.3"	1	SANYO
15	19.20086.001	LCD INVERTER FOR HIT 11.3"	1	AMBIT
16	23.42009.001	MICROPHONE	1	HOSIDEN
17	34.46829.001	HINGE (L) FOR 970	1	CEMA
18	34.46830.001	HINGE (R) FOR 970	1	CEMA
19	86.4A453.6R0	SCREW PAN M2.5*L6 NYLON	2	CASHI
20	47.46810.002	CUSHION SPACER(A) CR	2	S.Y.
21	40.46814.001	LCD FPC MYLAR	1	P.M.
22				
23				
24				
25				

65.46806.001 LCD 11.3" MODULE ASS'Y

DO NOT SCALE DRAWING

MODEL	970	NAME: LCD MODULE ASSEMBLY SANYO 11.3" SVGA STN	
DRN		MATERIAL	
DSN	TONY HSIAO	FINISH	MCS-050 — QTY 1
CKD		Acer Incorporated	
APPD			

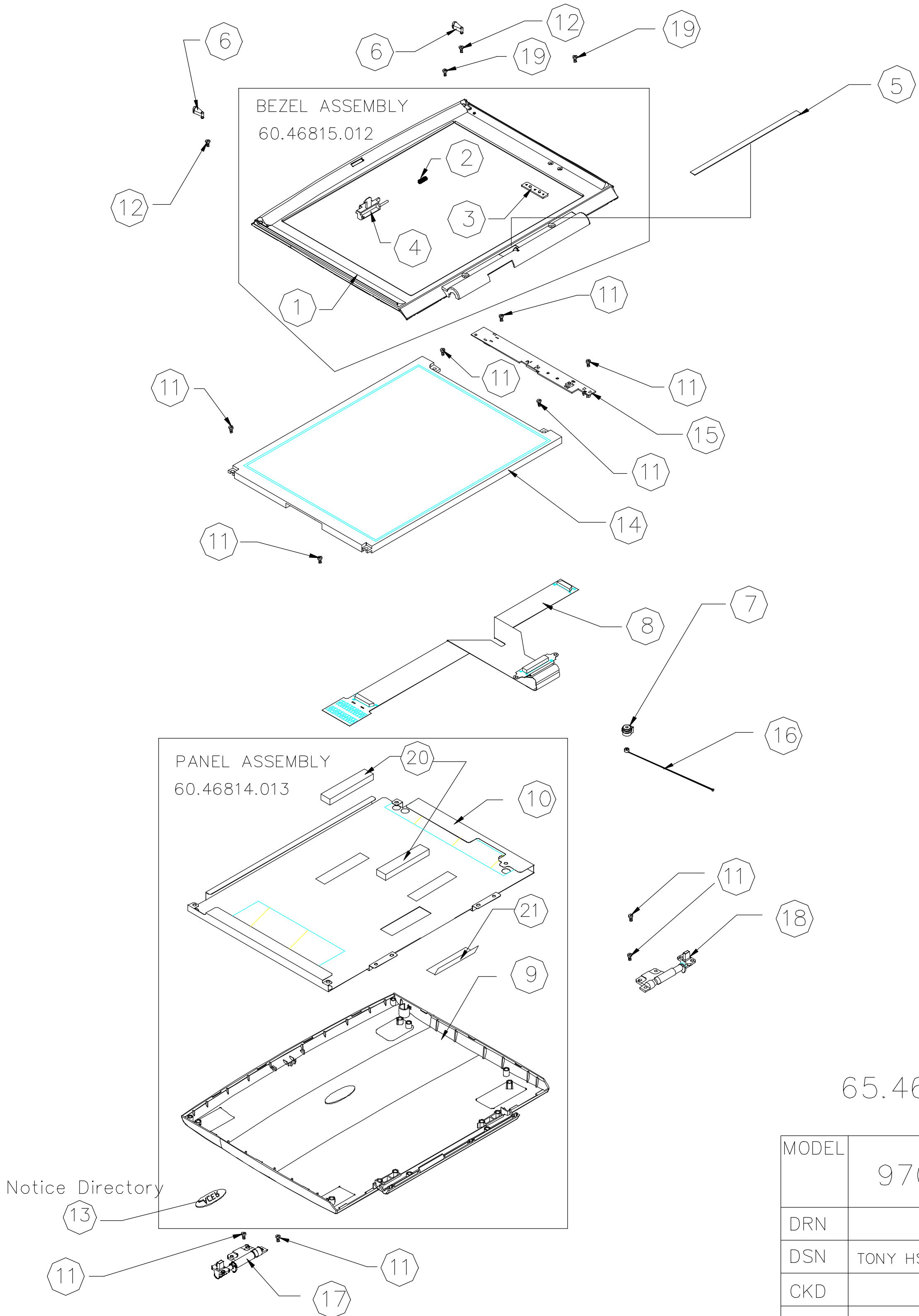
REV	DESCRIPTION	SIGN	DATE
2	add component		10/11 1996

DIM IN mm | SCALE | SHEET 1 OF 1

DRAWING NO. CD 65.46806.001

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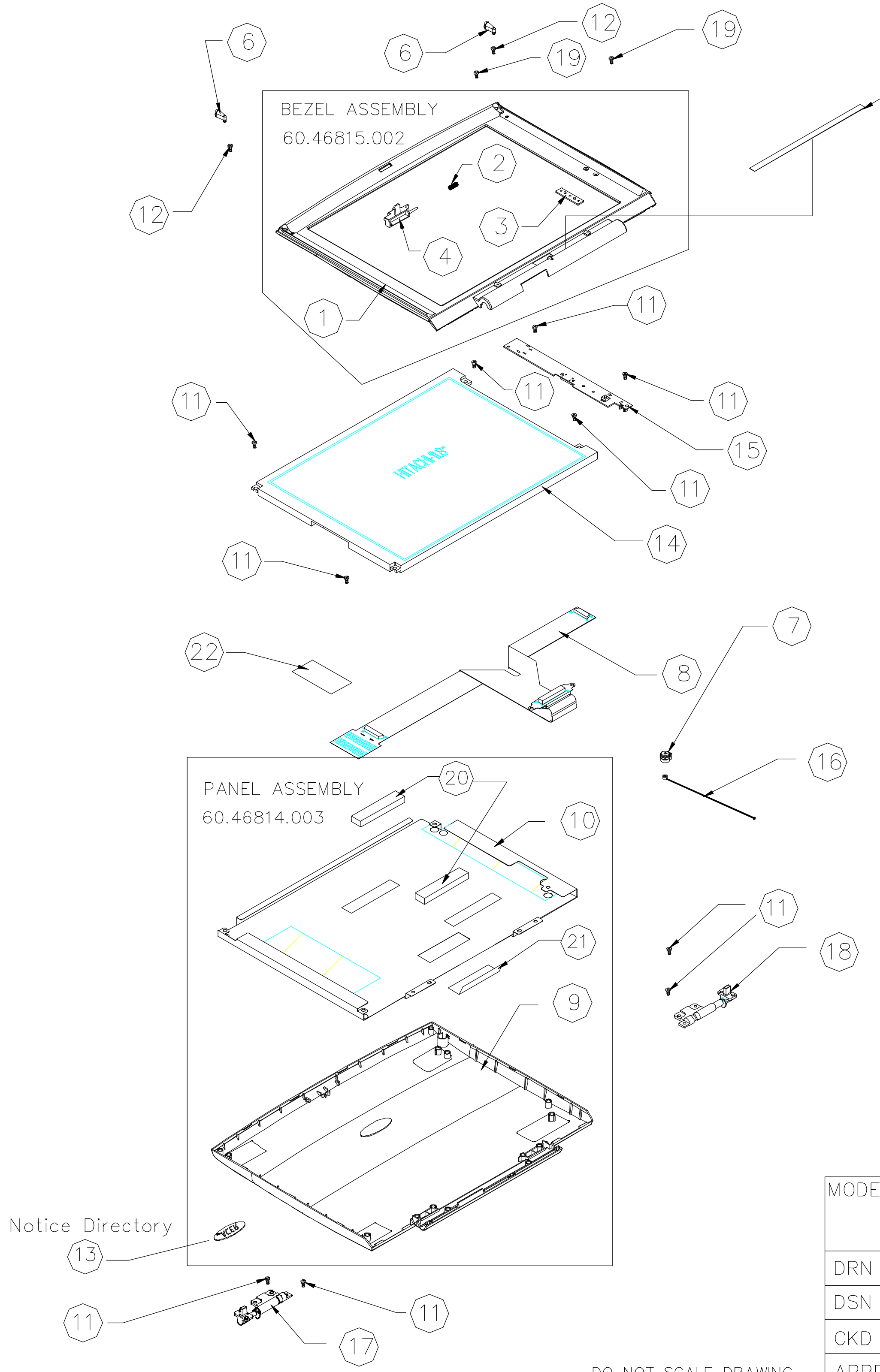
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03	42.46829.001	LED LENS,FOR POWER	1	S.J.
04	42.46828.001	LCD LATCH	1	S.J.
05	40.46805.001	ACER LOGO	1	S.Y.
06	47.46802.001	CUSHION BEZEL	2	P.M.
07	47.46803.001	CUSHION MICROPHONE	1	P.M.
08	50.46806.001	FPC LCD (HIT 11.3")	1	ADFLEX
09	41.46804.002	LCD PANEL FOR HIT 11.3"	1	S.J.
10	34.46831.002	EMI SHIELD FOR HIT 11.3"	1	S.Y.
11	86.4A453.6R0	SCREW PAN M2.5*L6 NYLON	10	CASHI
12	86.1A522.6R0	SCREW PAN MECH M2.0*L6	2	CASHI
13	31.46813.001	NAME PLATE, FOR ACER	1	OUDENSHA
14	56.07355.011	LCD SANYO SVGA STN 11.3"	1	HITACHI
15	19.20086.001	LCD INVERTER FOR SANYO 11.3"	1	AMBIT
16	23.42009.001	MICROPHONE	1	HOSIDEN
17	34.46829.001	HINGE (L) FOR 970	1	CEMA
18	34.46830.001	HINGE (R) FOR 970	1	CEMA
19	86.4A453.6R0	SCREW PAN M2.5*L6 NYLON	2	CASHI
20	47.46810.002	CUSHION SPACER(A) CR	2	S.Y.
21	40.46814.001	LCD FPC MYLAR	1	S.Y.
22				
23				
24				
25				



65.46806.011 LCD 11.3" MODULE ASS'Y

MODEL	970	NAME LCD MODULE ASSEMBLY HITACHI LMG9900ZWCC		1	add component		5/10 1996
DRN		MATERIAL		REV	DESCRIPTION	SIGN	DATE
DSN	TONY HSIAO	FINISH	MCS-050 QTY 1		DIM IN mm	SCALE	
CKD		Acer Incorporated			SHEET 1 OF 1		
APPD				DRAWING NO.	CD 65.46806.011		

DO NOT SCALE DRAWING



91.46801.001/65.46806.021 LCD MODULE ASSEMBLY(HITACHI 11.8")

No	Part No.	Description	Q'TY	Remark
01	41.46803.002	LCD BEZEL FOR HIT 11.8"	1	S.J.
02	34.47604.001	HOOK SPRING,EJ SPG	1	H.C.
03	42.46829.001	LED LENS,FOR POWER	1	S.J.
04	42.46828.001	LCD LATCH	1	S.J.
05	40.46805.001	ACER LOGO	1	S.Y.
06	47.46802.001	CUSHION BEZEL	2	P.M.
07	47.46803.001	CUSHION MICROPHONE	1	P.M.
08	50.46801.001	FPC LCD (HIT 11.8")	1	ADFLEX
09	41.46802.002	LCD PANEL FOR HIT 11.8"	1	S.J.
10	34.46815.002	EMI SHIELD FOR HIT 11.8"	1	S.Y.
11	86.4A453.6R0	SCREW PAN M2.5*L6 NYLON	10	CASHI
12	86.1A522.6R0	SCREW PAN MECH M2.0*L6	2	CASHI
13	31.46813.001	NAME PLATE, FOR ACER	1	OUDENSHA
14	56.07355.021	LCD HITACHI 11.8"	1	HITACHI
15	19.20086.001	LCD INVERTER FOR HIT 11.8"	1	AMBIT
16	23.42009.001	MICROPHONE	1	HOSIDEN
17	34.46829.001	HINGE (L) FOR 970	1	CEMA
18	34.46830.001	HINGE (R) FOR 970	1	CEMA
19	86.4A453.6R0	SCREW MECH M2.5*L6 NYLON	2	CASHI
20	47.46810.001	CUSHION SPACER(A) CR	2	S.Y.
21	40.46814.001	LCD FPC MYALR	1	P.M.
22	34.45222.001	COPPER TAPE	70mm	
23				
24				
25				

65.46806.021 LCD 11.8" MODULE ASS'Y

DO NOT SCALE DRAWING

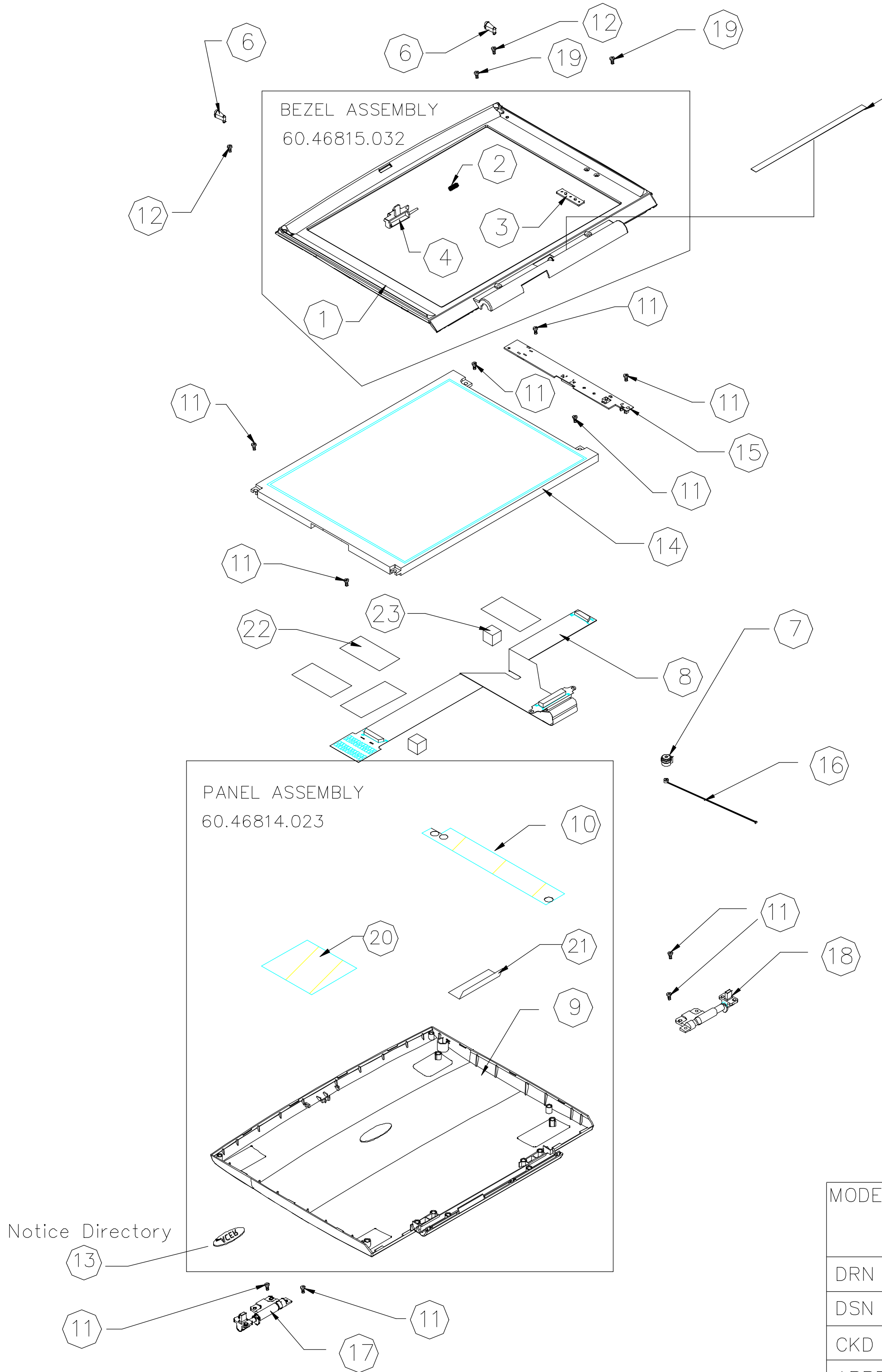
MODEL	970	NAME	LCD MODULE ASSEMBLY HITACHI TX30D01VC1CAA
DRN		MATERIAL	
DSN	TONY HSIAO	FINISH	MCS-050 QTY 1
CKD			Acer Acer Incorporated
APPD			

REV	DESCRIPTION	SIGN	DATE
1	add component		10/11 1996

DIM IN mm SCALE

SHEET 1 OF 1

DRAWING NO. CD 65.46806.021



91.46801.001/65.46806.041 LCD MODULE ASSEMBLY(IBMITSV50D 12.1")

No	Part No.	Description	Q'TY	Remark
01	41.46808.002	LCD BEZEL FOR IBM 12.1"	1	S.J.
02	34.47604.001	HOOK SPRING,EJ SPG	1	H.C.
03	42.46829.001	LED LENS,FOR POWER	1	S.J.
04	42.46828.001	LCD LATCH	1	S.J.
05	40.46805.001	ACER LOGO	1	S.Y.
06	47.46809.001	CUSHION BEZEL	2	P.M.
07	47.46803.001	CUSHION MICROPHONE	1	P.M.
08	50.46809.001	FPC LCD (IBM 12.1")	1	ADFLEX
09	41.46807.002	LCD PANEL FOR IBM 12.1"	1	S.J.
10	40.46815.001	INSUALTION FOR INVERTER	1	S.Y.
11	86.4A453.6R0	SCREW PAN M2.5*L6 NYLON	10	CASHI
12	86.1A553.6R0	SCREW PAN MECH M2.5*L6 NY	2	CASHI
13	31.46813.001	NAME PLATE, FOR ACER	1	OUDENSHA
14	56.07468.001	LCD IBM ITSV50D 12.1"	1	HITACHI
15	19.21030.041	LCD INVERTER FOR IBM 12.1"	1	AMBIT
16	23.42009.001	MICROPHONE	1	HOSIDEN
17	34.46829.001	HINGE (L) FOR 970	1	CEMA
18	34.46830.001	HINGE (R) FOR 970	1	CEMA
19	86.4A453.6R0	SCREW MECH M2.5*L6 NYLON	2	CASHI
20	40.46816.001	INSULATION FOR FPC	1	S.Y.
21	40.46814.001	LCD FPC MYALR	1	P.M.
22	34.45222.001	COPPER TAPE	270mm	
23	42.45270.001	GASKET 71TS10-10*10	20mm	
24				
25				

65.46806.041 LCD 12.1" MODULE ASS'Y

DO NOT SCALE DRAWING

MODEL	970	NAME LCD MODULE ASSEMBLY IBM ITSV50D		1	add component		10/11 1996
DRN		MATERIAL		REV	DESCRIPTION	SIGN	DATE
DSN	TONY HSIAO	FINISH	MCS-050	QTY 1	DIM IN mm	SCALE	
CKD		Acer Incorporated			SHEET 1 OF 1		
APPD				DRAWING NO.	CD 65.46806.041		

Spare Parts

This appendix lists the spare parts of the notebook.

Table C-1 Spare Parts List

No.	Part Name	Part No.[1]	Comment / Location	Qty.[2]
Mechanical & Modules				
1	CONVERTER DC-DC T62.036.C 970	19.20084.011		1
2	ADT 90-264V 65W ZVC70 970	25.10043.001		1
3	CORD SPT-2 #18*2C 7A125V1830MM	27.01618.001		50
4	STANDOFF HEX M2.5*0.45 9MM	34.42801.001		50
5	FRAME KEYBOARD SECC 970	34.46805.001		50
6	COVER BATTERY PC+10%GF 050 970	42.46801.001		50
7	RAIL MODULE MYLON66 050 970	42.46821.001		50
8	COVER MIDDLE PC+10%GF 050 970	42.46822.001		50
9	CASE UP FDD PC+GF 050 970	42.46846.001		5
10	CABLE ASSY FDD 52P 970	50.46802.001		5
11	ASSY CD-ROM CABLE 52P 970	50.46804.001		5
12	CABLE ASSY FPC TOUCH PAD 970	50.46808.001		5
13	"FDD 1.44 3.5"" D353F2 000(3MODE"	56.01051.071	(MITSUMI)	1
14	HDD 1440MB IBM/DMCA-21440 ATA	56.02921.001		1
15	CD DRV TOSH/XM1402B 6X AT	56.10071.081		1
16	TOUCHPAD SYNAPTIC/TM1002SC 970	56.17468.001		1
17	ASSY CHASSIS MAIN 970	60.46803.021		1
18	ASSY COVER R HINGE 050 970	60.46805.001		5
19	ASSY COVER L HINGE 050 970	60.46805.011		5
20	ASSY COVER HDD 970	60.46805.021		50
21	ASSY CASE UPPER 050 970	60.46807.001		1
22	ASSY CASE LOWER 050 970	60.46808.001		1
23	ASSY KB COVER 050 970	60.46816.001		5
24	ASSY BTY PACK 10.8V BTP-S31	60.46818.011		1

[1] Part numbers are subject to change without notice. Contact the Acer spare parts department for updates.

[2] Minimum ordering quantity.

Table C-1 Spare Parts List

No.	Part Name	Part No.[1]	Comment / Location	Qty.[2]
25	ASSY CD ROM BEZEL 050 970	60.46821.001		5
26	ASSY FDD L-CASE 050 970	60.46822.001		5
27	KB-84 KEY KAS1901-0111R US	90.46807.001		1
11.3", Hitachi LCD Kit				
1	INVERTER T62.039.C 970	19.20086.001		1
2	MICROPHONE 54DB KUC8723-030839	23.42009.001		5
3	HINGE (L) AL 970	34.46829.001		5
4	HINGE (R) AL 970	34.46830.001		5
5	"CABLE ASSY FPC(11.3""HIT)970"	50.46806.001		1
6	"LCD LMG9930ZWCC HIT 11.3""SVGA"	56.07469.091		1
7	ASSY LCD PNL(11.3HIT)050 970	60.46814.011		5
8	"ASSY LCD BZL(11.3"")050 970"	60.46815.011		5
11.8", Hitachi LCD Kit				
1	INVERTER T62.039.C 970	19.20086.001		1
2	MICROPHONE 54DB KUC8723-030839	23.42009.001		5
3	HINGE (L) AL 970	34.46829.001		5
4	HINGE (R) AL 970	34.46830.001		5
5	CABLE ASSY 80P FPC 970	50.46801.001		1
6	LCDM TX30D01VC1CAA 11.8TFT HIT	56.07355.021		1
7	ASSY LCD PNL(11.8HIT) 050 970	60.46814.001		5
8	"ASSY LCD BZL(11.8"")050 970"	60.46815.001		5
Main board				
1	IC CPU P54CSLM-133 2.9V	01.IP54S.D3T	U1	1
2	CHOKE 9UH A-1004-09	19.40116.001	L5	5
3	CONN D FML 3R15P RT D0.762	20.20076.015	CN6	50
4	CONN D FML 2R25P RT D1.38	20.20077.025	CN13	50
5	CONN EDGE SMD FML 120[ST D0.8	20.C0004.120	"CN7,10"	5
6	HEAD ML 2R 44P ST D2 L3.5	21.60063.222	CN5	50
7	CONNECTOR RECEPT 3R240P RT(AMP	21.80016.240	CN9	5
8	CONN D SMD 52P RT D0.635 H11	21.A0006.052	CN11	5
9	HEADER SMD FML 2R20P ST D2 4S	21.E0004.210	"CN19,20"	50
10	CONN CTR SMD ML 160P ST D0.5	21.F0009.160	CN12	5
11	CONN CTR SMD FML 40P ST D0.5	21.F0010.040	CN18	50
12	CONN CTR SMD FML 160P ST D0.5	21.F0010.160	CN8	5
13	SKT MINI-DIN FML 6P RT SHIELD	22.10021.011	CN15	50

Table C-1 Spare Parts List

No.	Part Name	Part No.[1]	Comment / Location	Qty.[2]
14	SKT PHONE JACK 5P3C MOJ-B27-B	22.10139.001	"CN2,3"	50
15	SKT PHONE JACK FML 6P4C RT	22.10177.001	CN4	50
16	SKT DC 8A 20V TCP7631-01-0201	22.10179.001	CN16	50
17	SW PUSH SPDT 0.05A 48V RT	22.40091.001	SW1	5
18	BATTERY LI 3V BR1225-T2V	23.20004.014	BT1	50
19	FILTER EMI BNX002-01 50V 10A	24.20058.001	T1	5
20	CABLE ASSY FPC 44P 43MM	50.42003.002	(HDD CABLE)	5
21	MAIN BD W/O CPU 0MB 970	55.46801.001		1
22	TCP CPU BD 133MHZ 970	55.46802.011		1
23	DIMM EDO 16MB 3.3V 60NS	55.46804.011		1
24	SIR MODULE TEMIC TFDS3000	56.15468.001	U1	5
25	ASSY BRACKET I/O 970	60.46801.001		5
26	SKT IC PLCC 68P SMD	62.10004.068	U40	5
27	SKT DIMM 144P C-316310-1	62.10017.144	"SI1,2"	5
28	IC PCI-IDE CTRL PCI0643 TQFP	71.00643.00G	U38	5
29	IC U SUPERVISORY MAX708ESA S08	71.00708.00A	"U52,55"	5
30	IC CLK GEN MK1438-01RTR SSOP	71.01438.00I	U5	5
31	IC AUDIO CHIP ESS1688 PQFP100P	71.01688.00E	U8	1
32	IC RTC BQ3285E SSOP 24P	71.03285.00I	U9	5
33	IC BUS SWITCH QS32*L384 VSOP48	71.32384.00N	U12	5
34	IC PCI SYS CTRL PT86C521 VQFP	71.86521.00V	U30	1
35	IC DATA PATH PT86C522 VQFP208P	71.86522.00V	U41	1
36	IC PCI/ISA BRI PT86C523 VQFP	71.86523.00V	U29	1
37	IC SUPER I/O PC87336VLJ QFP100	71.87336.00E	U24	5
38	IC UCTRL 87C552 8BIT PLCC 68P	71.87552.00C	U40	1
39	IC EPROM 28F002BX-T 2M TSOP40P	72.28002.009	U23	1
40	IC SRAM KM732V588 32K*32 PQFP	72.32588.005	"U31,32"	5
41	IC SRAM 7C1399 15NS 32K*8 SOJ	72.71399.23B	U35	5
42	IC EPROM 87C51SLAH 16K(OTP)5V	72.87C51.16M	U16	1
43	IC PAL 16V8Z-15JI PLCC 20P	73.16V8Z.BD3	U28	1
44	IC DC/DC CONVERT MAX797 SO-W	74.00797.032	U56	5
45	IC TRANSCEVR MAX211ECAI SSOP28	74.0211E.0F9	U48	5
46	IC AUDIO AMP. LM4861 SO-N 8P	74.04861.011	"U10,11"	5
47	IC ANALOG SW.PI5C3126 SO-W	74.53126.091	U4	5
Media board				

Table C-1 Spare Parts List

No.	Part Name	Part No.[1]	Comment / Location	Qty.[2]
1	CONN CTR SMD FML 22P ST D0.8	20.F0002.022	CN5	50
2	CONN CTR SMD PLUG 80P D0.8	21.F0012.080	CN6	5
3	CONNECTOR CTR SMD ML 120P ST	21.F0014.120	"CN8,10"	5
4	CONN CARD PUSH C-11093 EJECT	21.H0007.001		1
5	MEDIO BOARD 970	55.46803.001		1
6	SKT PCMCIA 152P C-917573 SMD	62.10018.152	CN9	5
7	IC VGA CTRL NM2090 TQFP 176P	71.02090.00G	U24	1
8	IC PWR INTF.SW TPS2202AIDF SOP	71.02202.00N	U28	5
9	IC MODEM DIGI R6684-17 PLCC68P	71.06684.00C	U19	1
10	IC MDP R6693-14 PQFP 100P	71.06693.00E	U3	1
11	IC MCU R6723-12 PQFP 100P	71.06723.A0E	U17	1
12	IC PCMCIA CL-PD6730-VC VQFP	71.06730.00V	U27	1
13	IC EEPROM ST24C02A 256K*8 SO-N	72.02402.001	UX1	50
14	IC SRAM MCM6206 15NS 32K*8 SOJ	72.06206.23B	U18	5
15	IC EEPRM 27C010L-45TC 128K*8	72.27010.189	U16	5
Optional Items				
1	ADT 90-264V 65W ZVC70 970	25.10043.001		1
2	S.A. 25P(D CONN)2464 #26 120CM	50.30014.001	(FILE TRANS. CABLE)	5
3	C.A 25/52P 300MM EXT FDD 970	50.46810.001		1
4	C.A KB&MOUSE Y 200MM 970	50.46812.001		5
5	DIMM EDO 8MB 3.3V 60NS	55.46804.001		1
6	DIMM EDO 16MB 3.3V 60NS	55.46804.011		1
7	DIMM EDO 32MB 3.3V 60NS 4K	55.46804.021		1
8	FDD-931	91.46805.001		1
9	FDD-963	91.46805.002		1
10	BTP-S31	91.46828.001		1
11	BTP-S61	91.46828.003		1
12	ADS-131	91.46828.021		1
13	ADS-160	91.46828.022		1
14	CDR-630	91.46837.001		1
15	CDR-664	91.46837.003		1

Schematics

The Appendix D has three sections for presenting system board, media board, and CPU board schematics.

This section shows the **system board** schematic diagrams of the notebook.

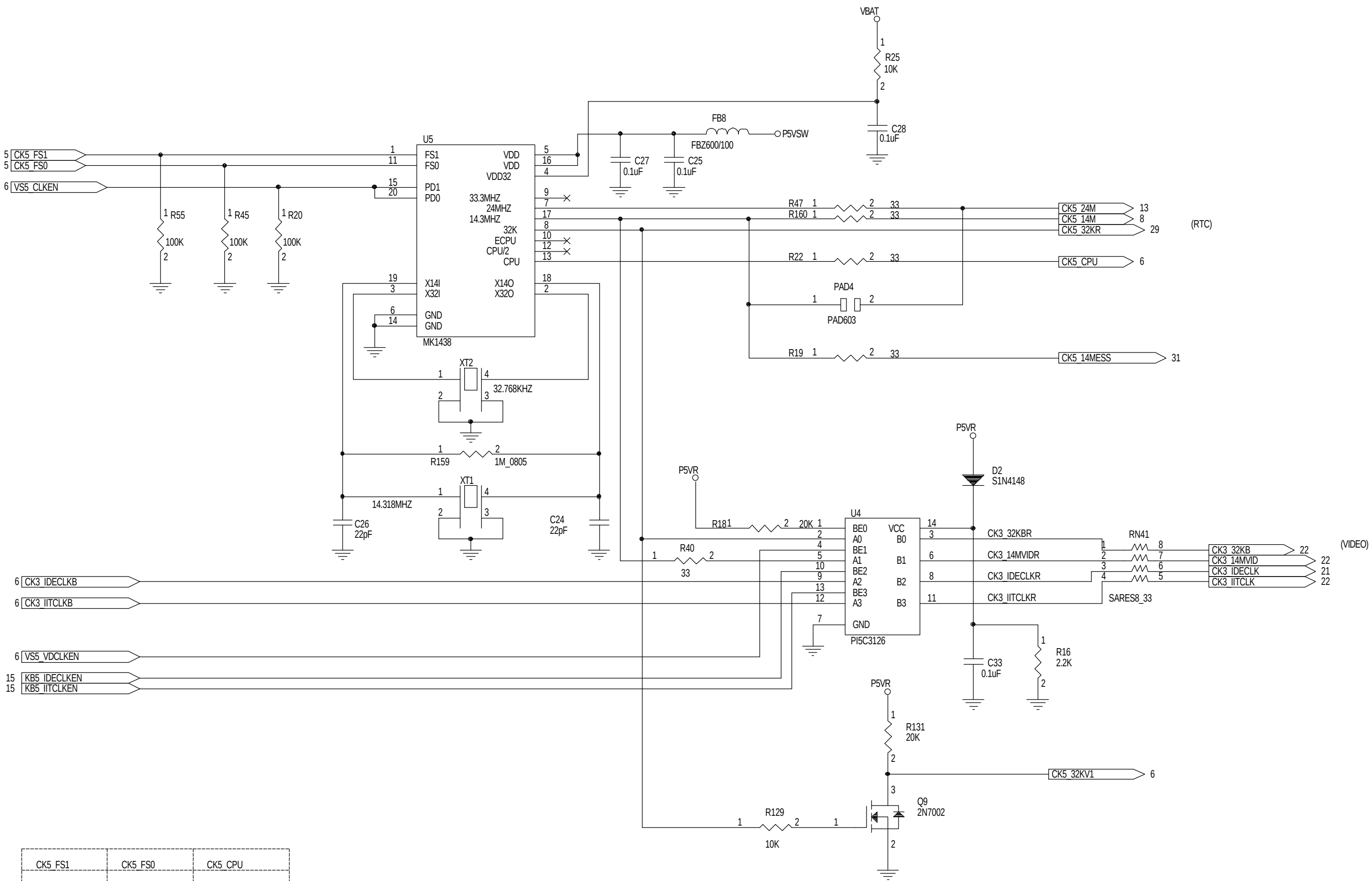
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PROJECT MARS SYSTEM BOARD

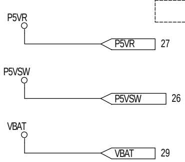
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PAGE SYSTEM FUNCTION DESCRIPTION

PAGE SYSTEM FUNCTION DESCRIPTION

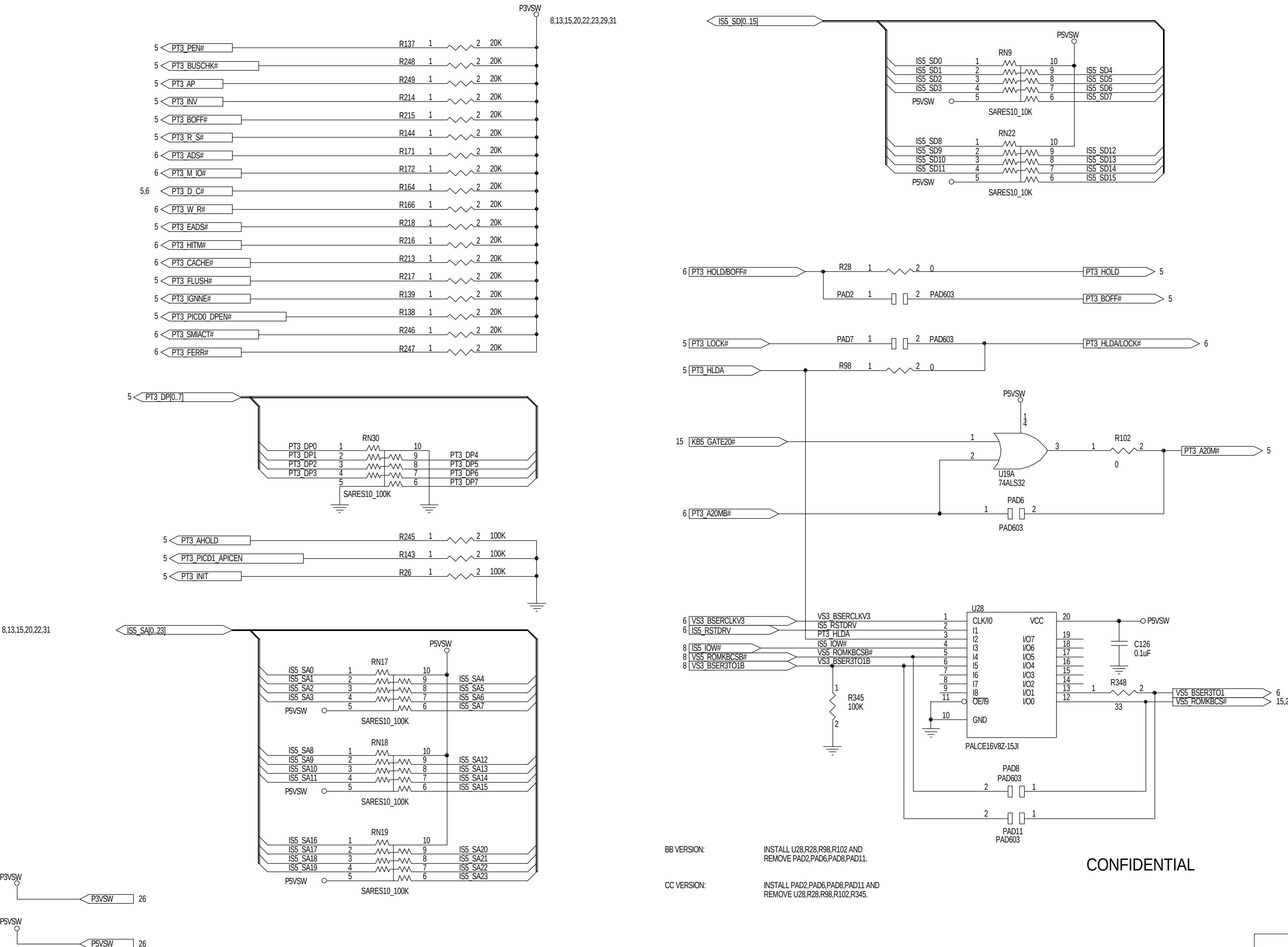


CK5_FS1	CK5_FS0	CK5_CPU
0	0	33.33MHz
0	1	50.00MHz
1	0	66.66MHz
1	1	60.00MHz



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ACER ADVANCED LABS,Inc.	
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Date: May 15, 1996	Sheet 2 of

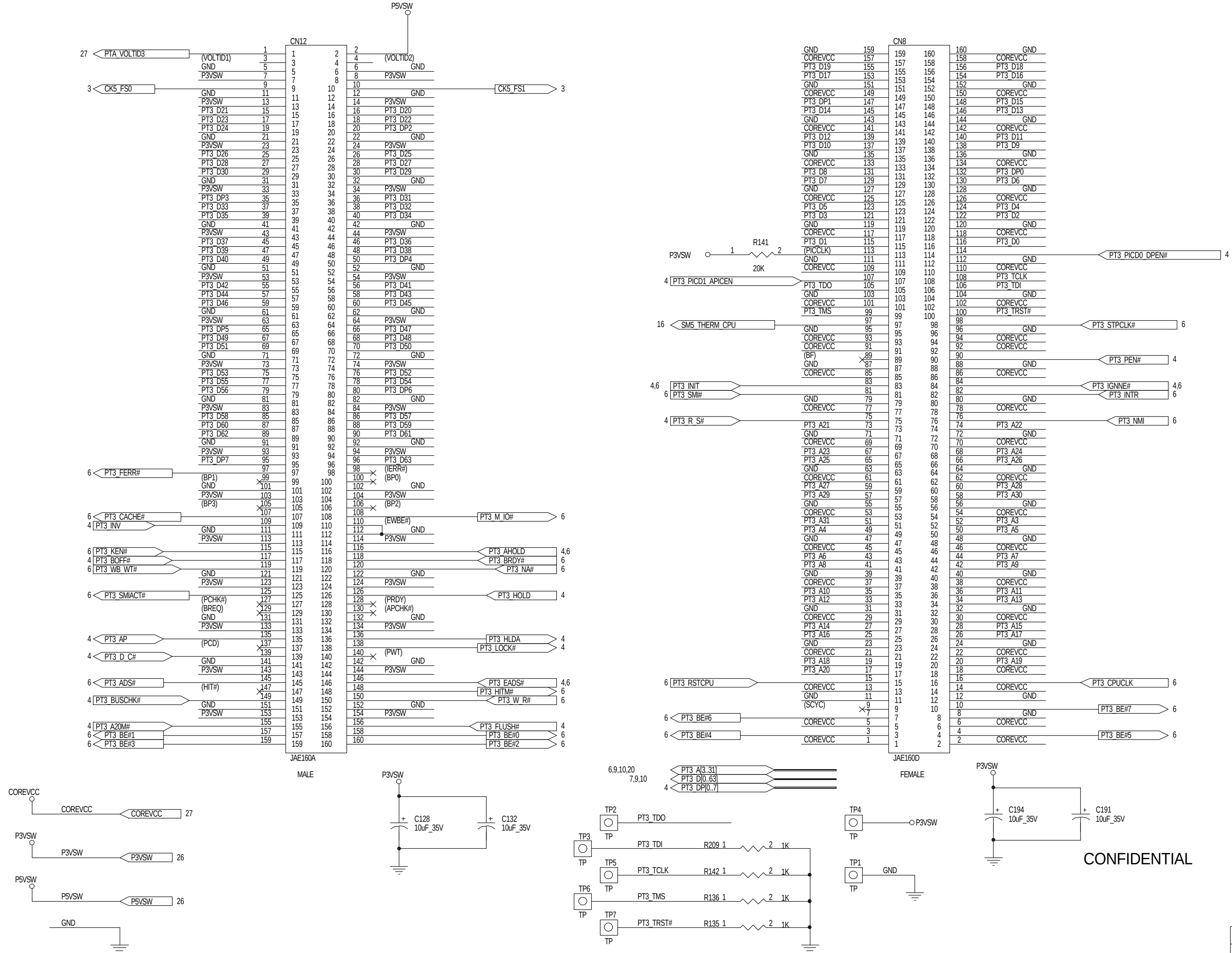


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CC VERSION: INSTALL PAD2,PAD6,PAD8,PAD11 AND REMOVE U28,R28,R98,R102,R345.

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Size A3	Document Number
Date: May 15, 1996	Sheet 4 of



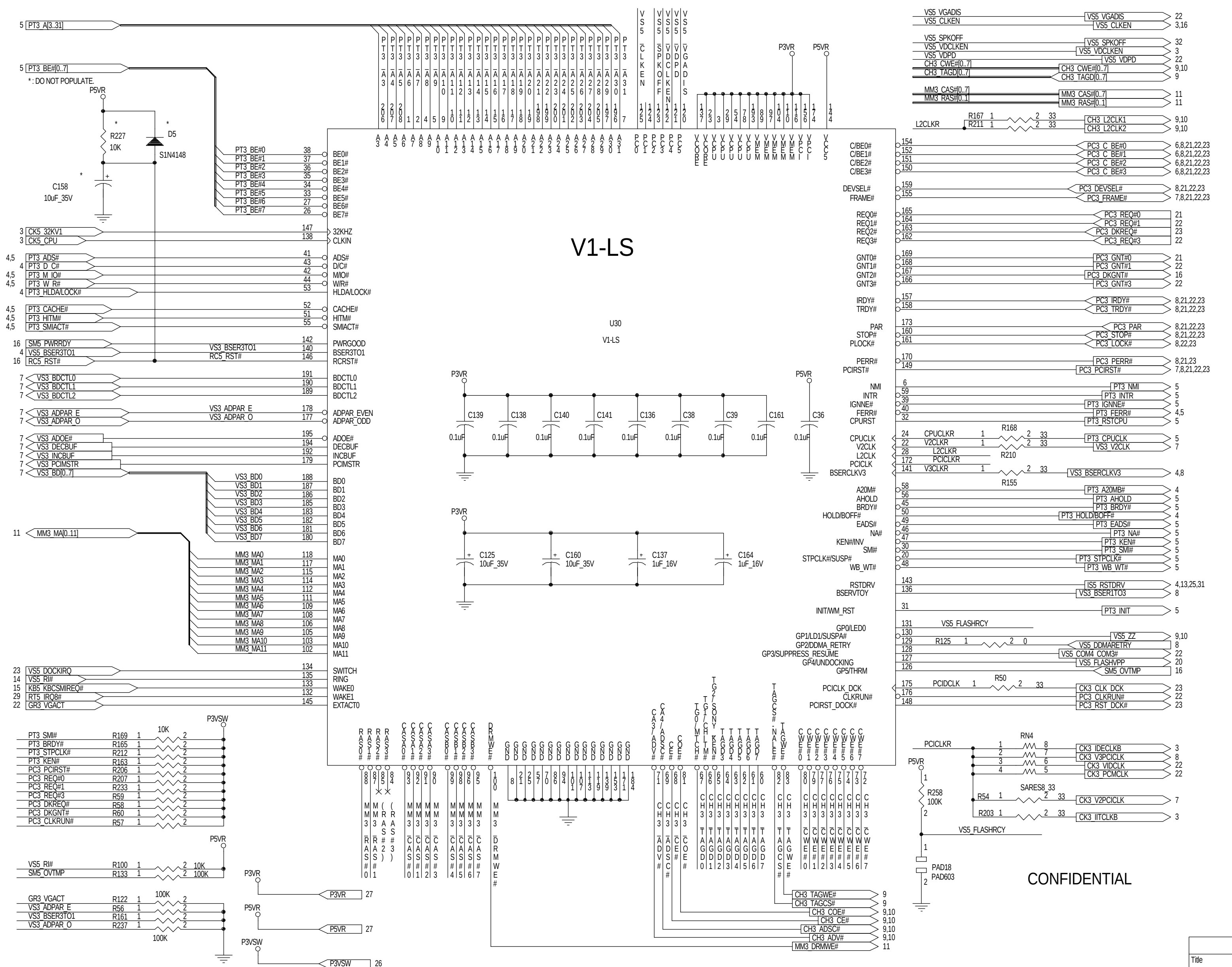
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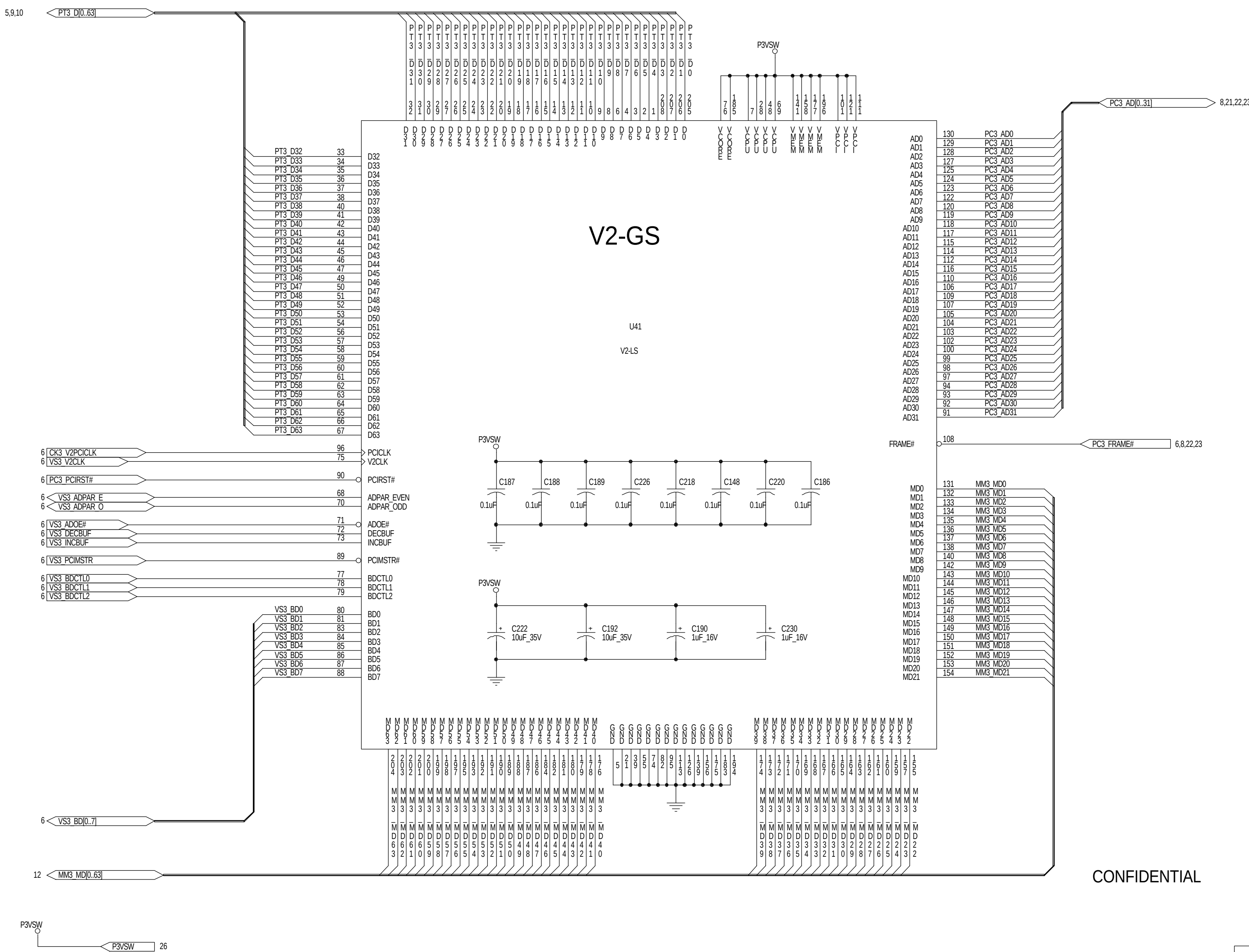
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Date: May 8, 1996 | Sheet 5 of



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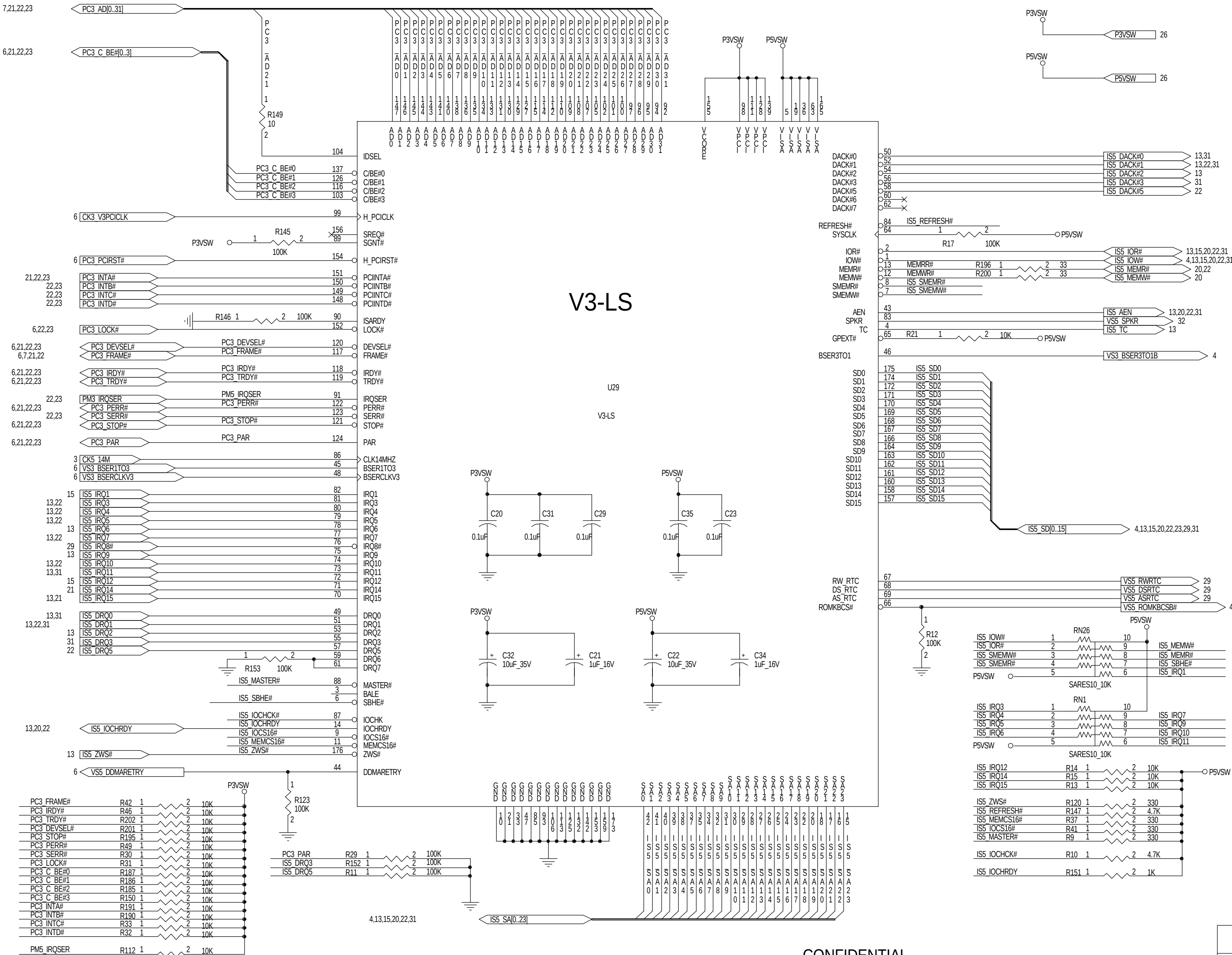


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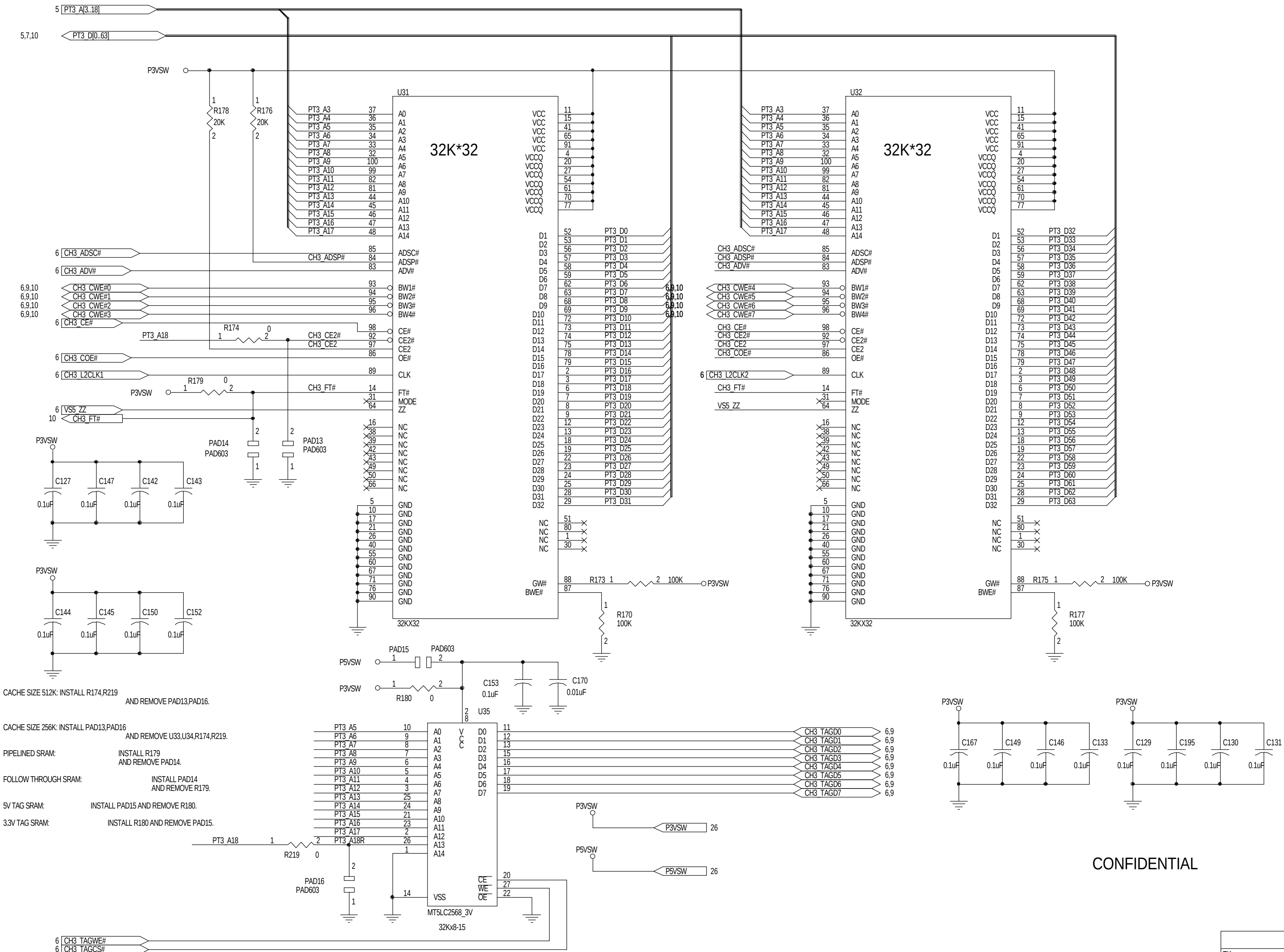
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Date: May 8, 1996 | Sheet 7 of



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ACER ADVANCED LABS			
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Size A3	Document Number V3-GS		
Date: May 8, 1996		Sheet 8	of 32



CACHE SIZE 512K: INSTALL R174,R219
AND REMOVE PAD13,PAD16.

CACHE SIZE 256K: INSTALL PAD13,PAD16
AND REMOVE U33,U34,R174,R219.

PIPELINED SRAM: INSTALL R179
AND REMOVE PAD14.

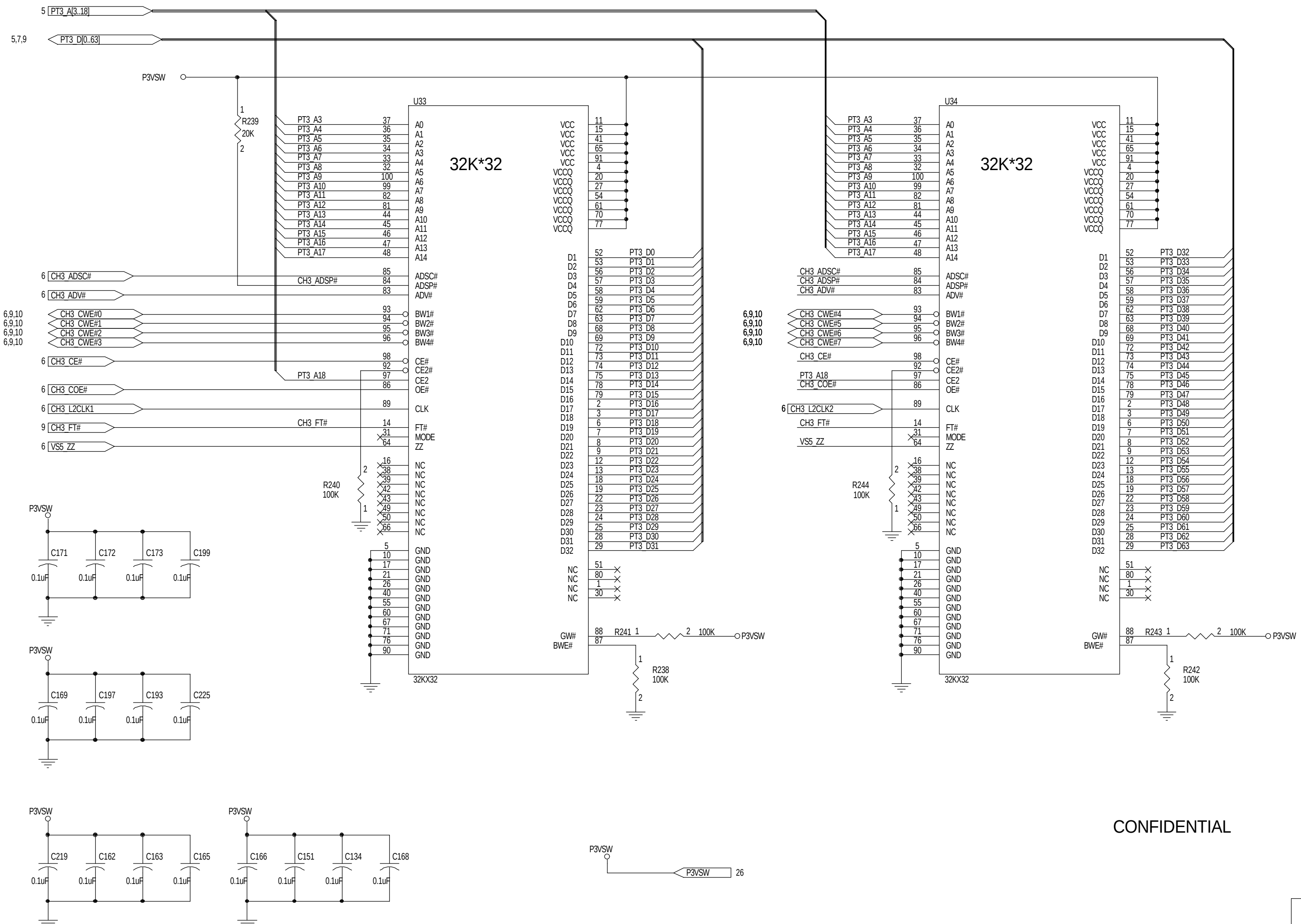
FOLLOW THROUGH SRAM: INSTALL PAD14
AND REMOVE R179.

5V TAG SRAM: INSTALL PAD15 AND REMOVE R180.

3.3V TAG SRAM: INSTALL R180 AND REMOVE PAD15.

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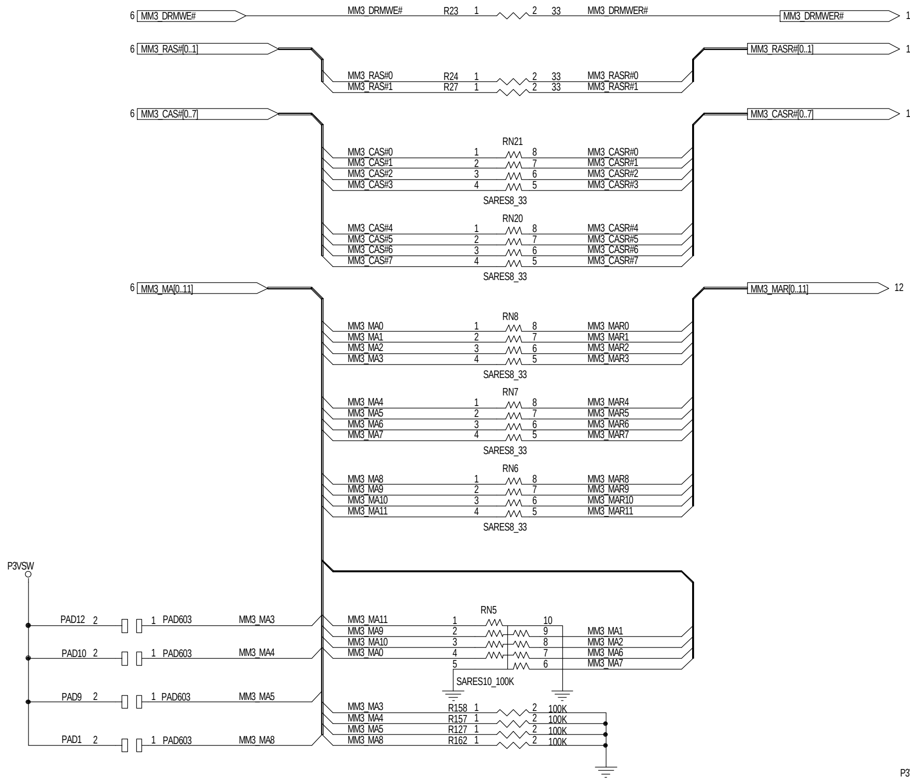
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Size: A3

Document Number: SYNC CACHE

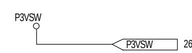
Date: May 8, 1996 | Sheet 10 of



MA3,MA4,MA5:TO ADJUST CLOCK SKEW

VERSION	BB	CC
MA0	LOW	LOW
MA1	LOW	LOW
MA2	LOW	LOW
MA3	LOW	LOW
MA4	LOW	LOW
MA5	LOW	LOW
MA6	LOW	LOW
MA7	LOW	LOW
MA8	LOW	HIGH
MA9	LOW	LOW
MA10	LOW	LOW
MA11	LOW	LOW

CONFIG SETTINGS



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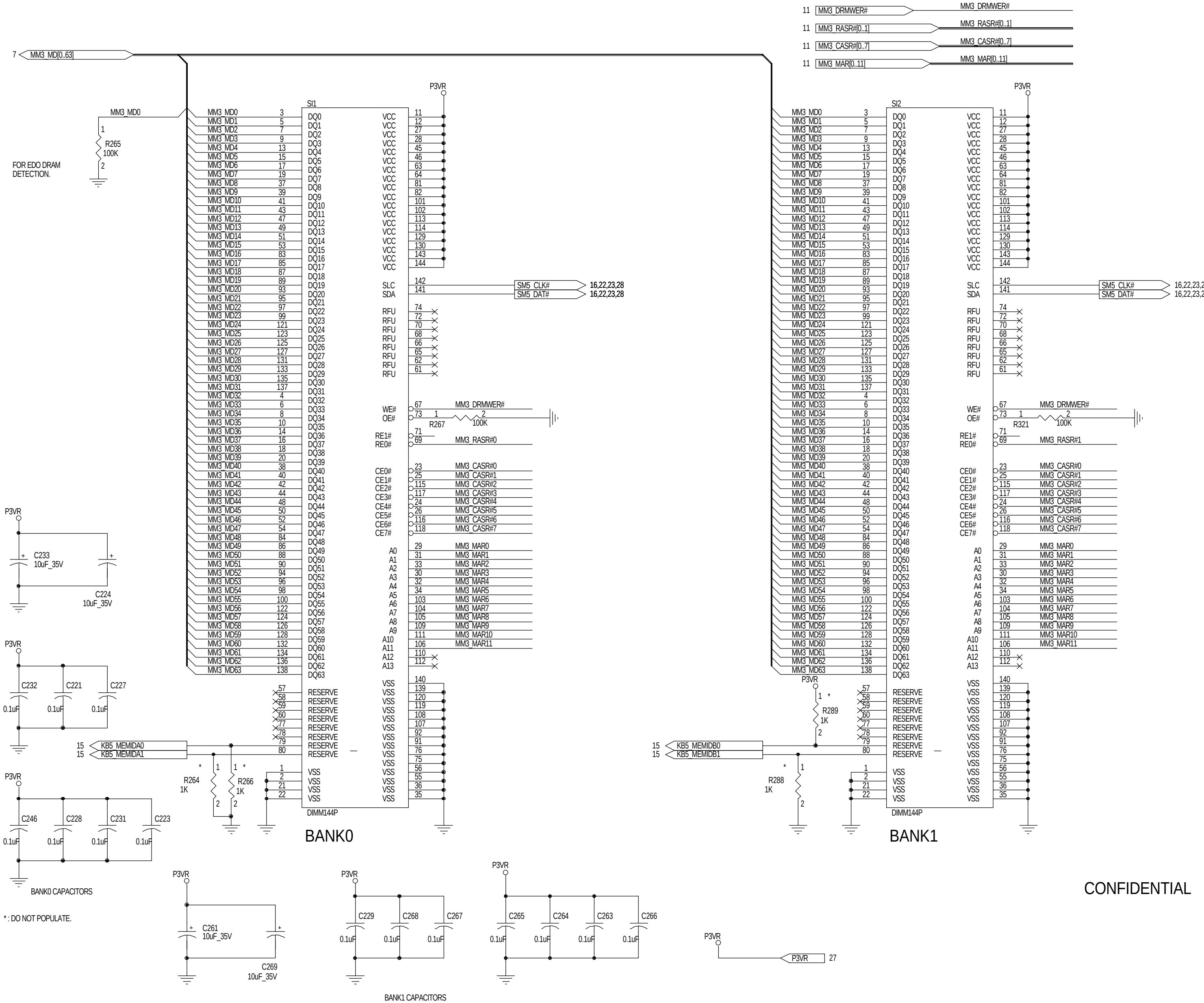
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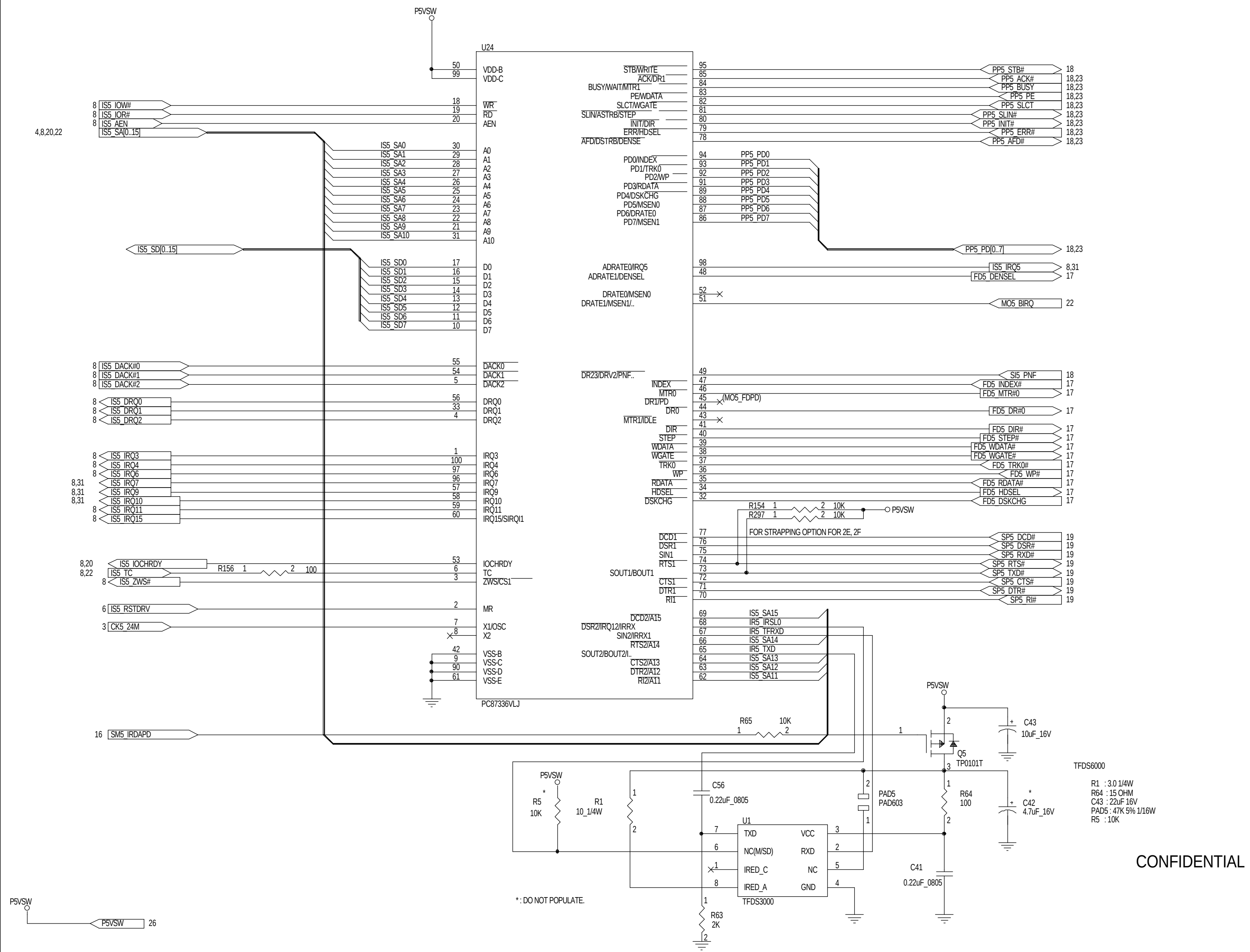
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Date: May 8, 1996 Sheet 11 of



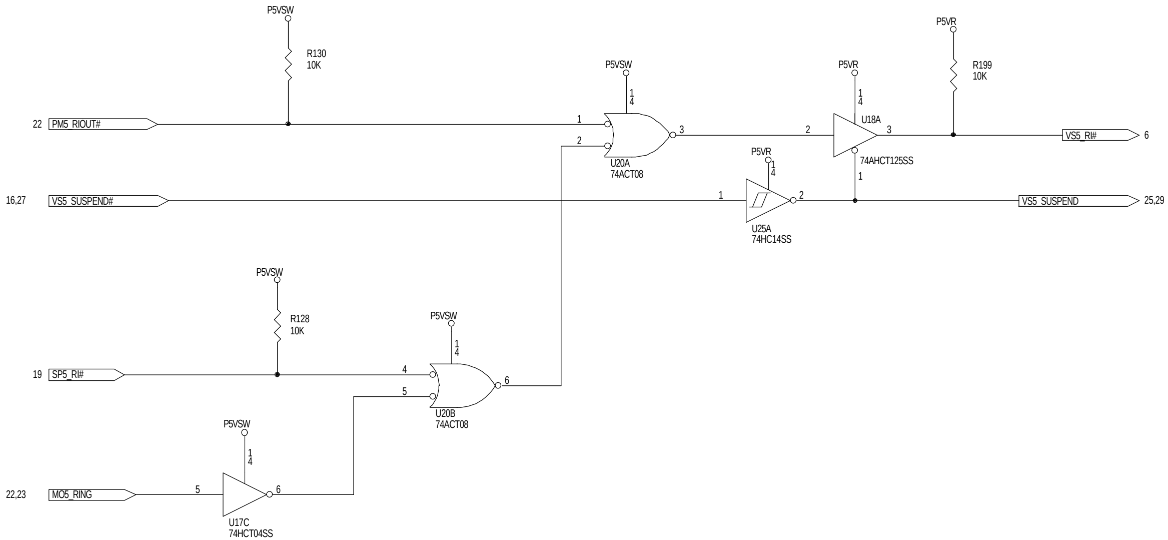
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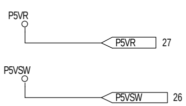
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Size A3	Document Number



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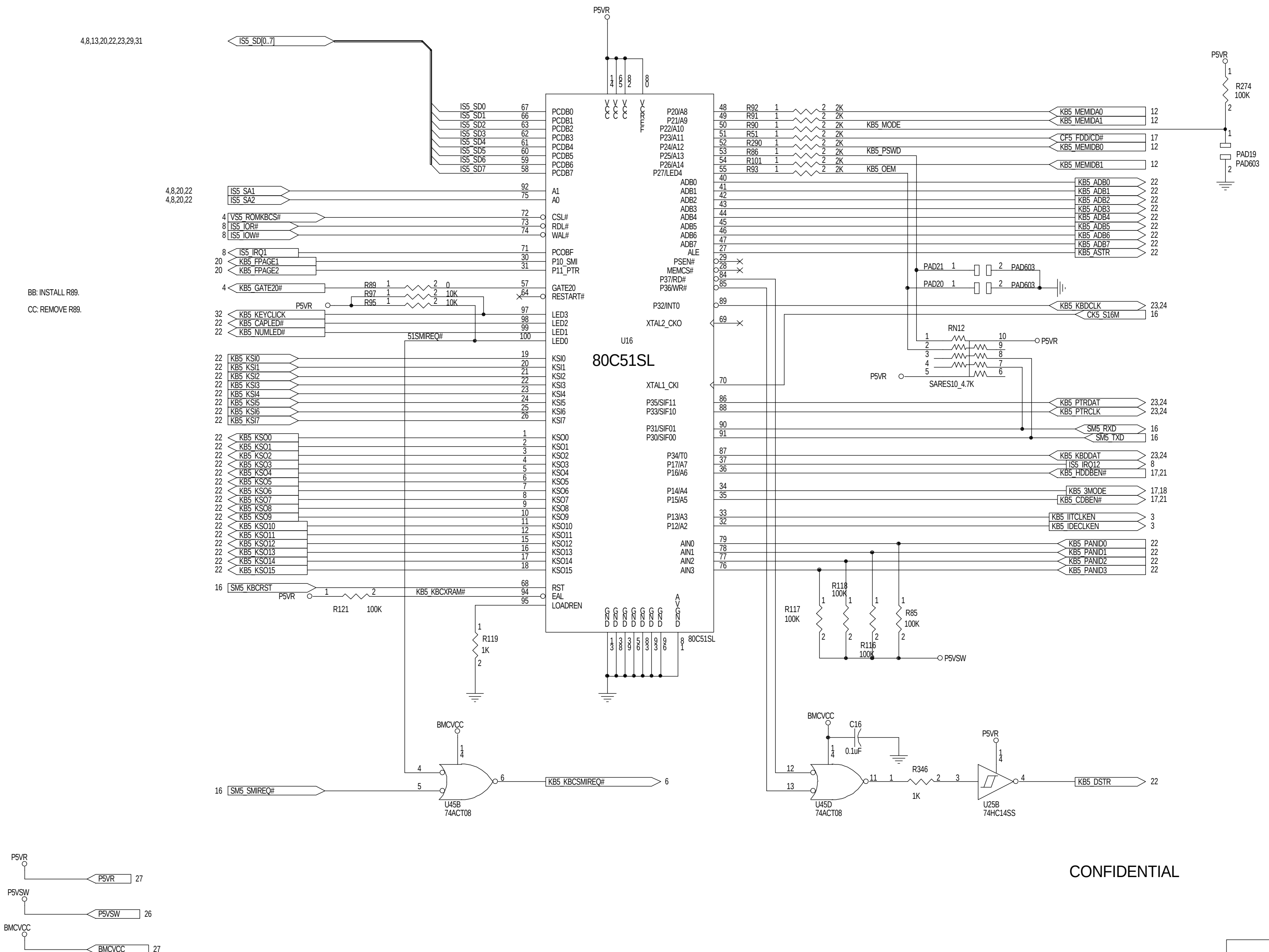
ACER ADVANCED LABS		
Title	PROJECT MARS	
Size A3	Document Number SUPER I/O CONTROLLER	
Date: May 22, 1996	Sheet 12	of





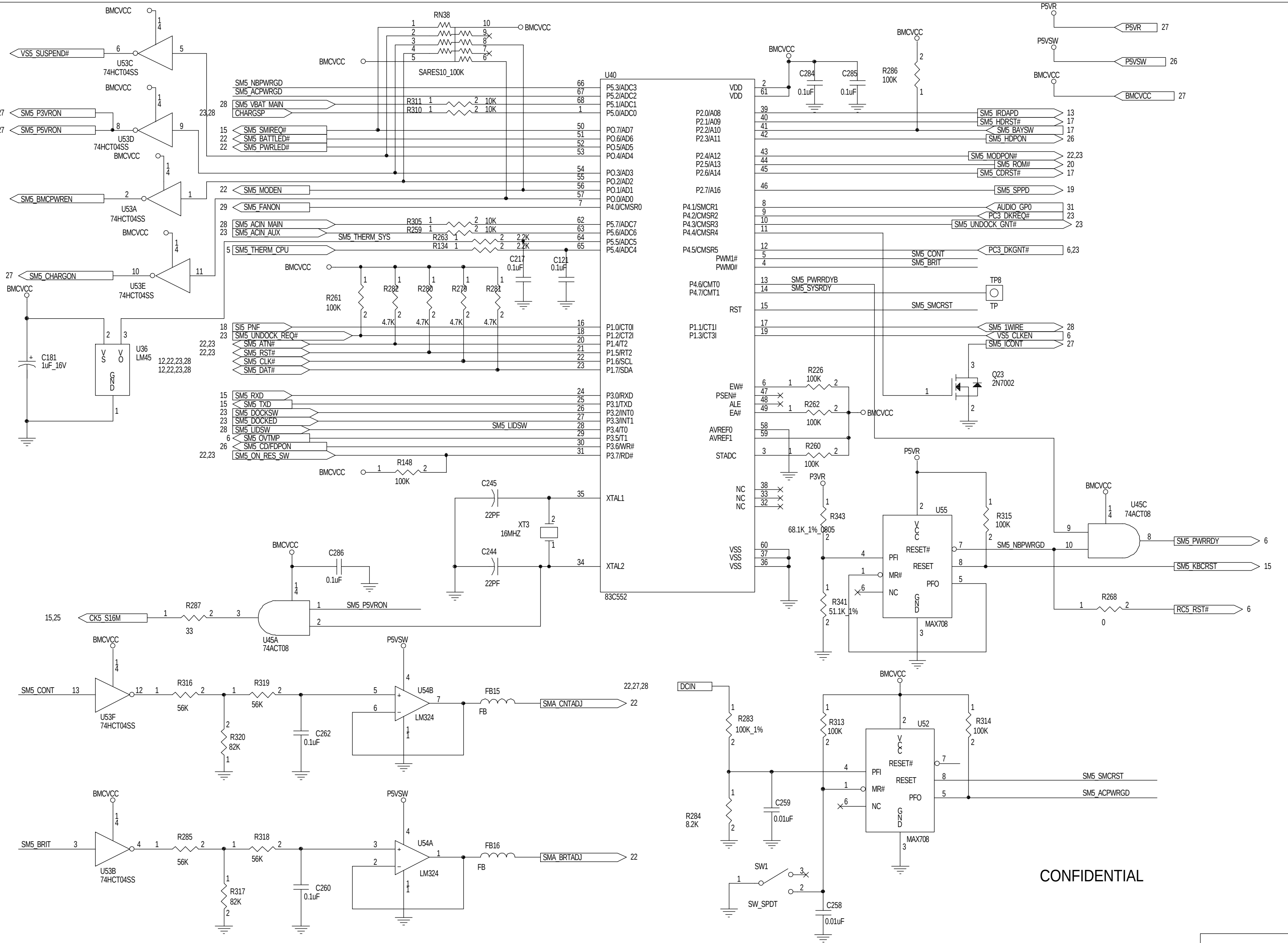
CONFIDENTIAL

ACER ADVANCED LABS	
Title	PROJECT MARS
Size A3	Document Number RI# INTERFACE LOGIC



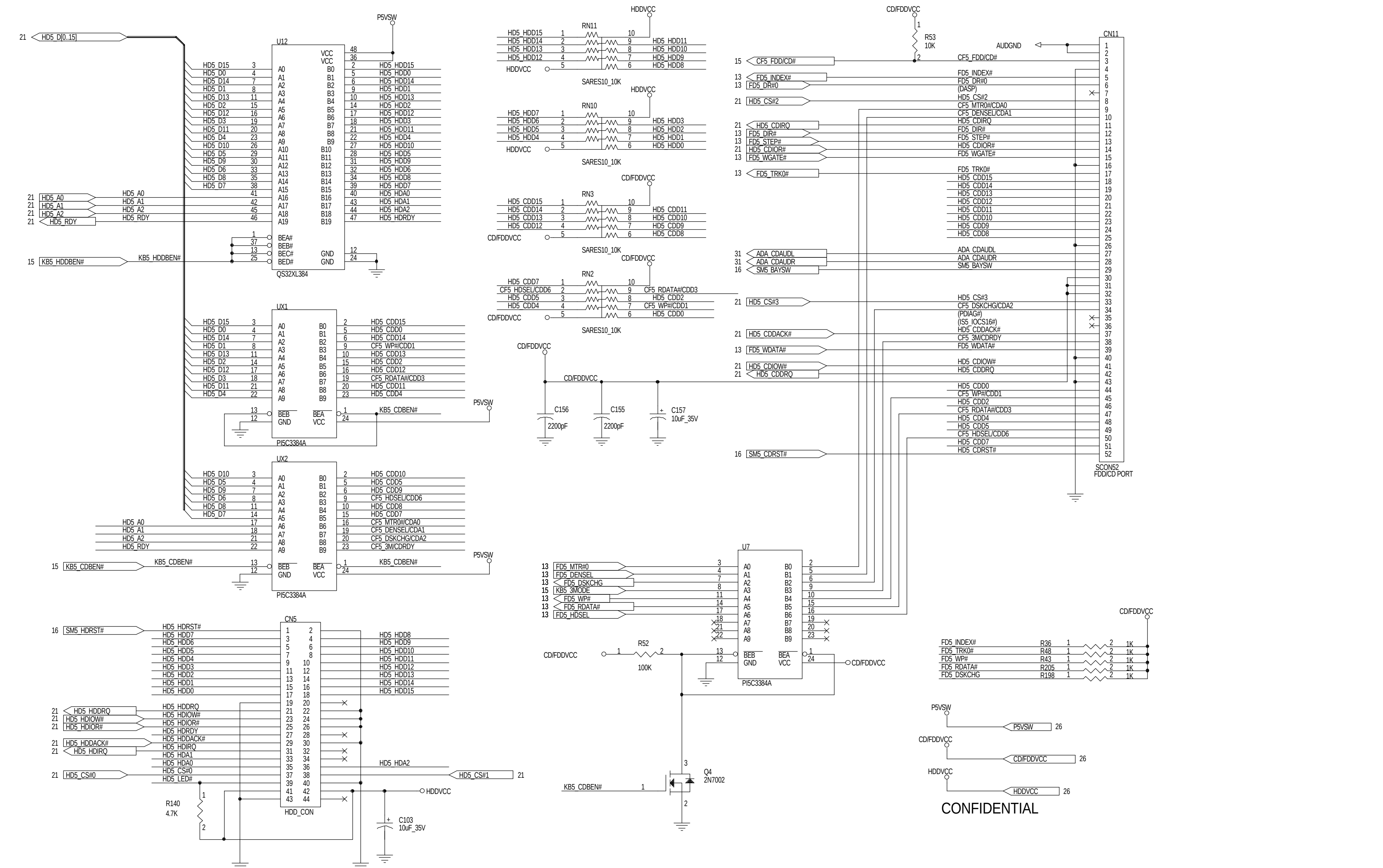
CONFIDENTIAL

ACER ADVANCED LABS	
Title	PROJECT MARS
Size A3	Document Number: KEYBOARD CONTROLLER
Date: May 22, 1996	Sheet 15 of



CONFIDENTIAL

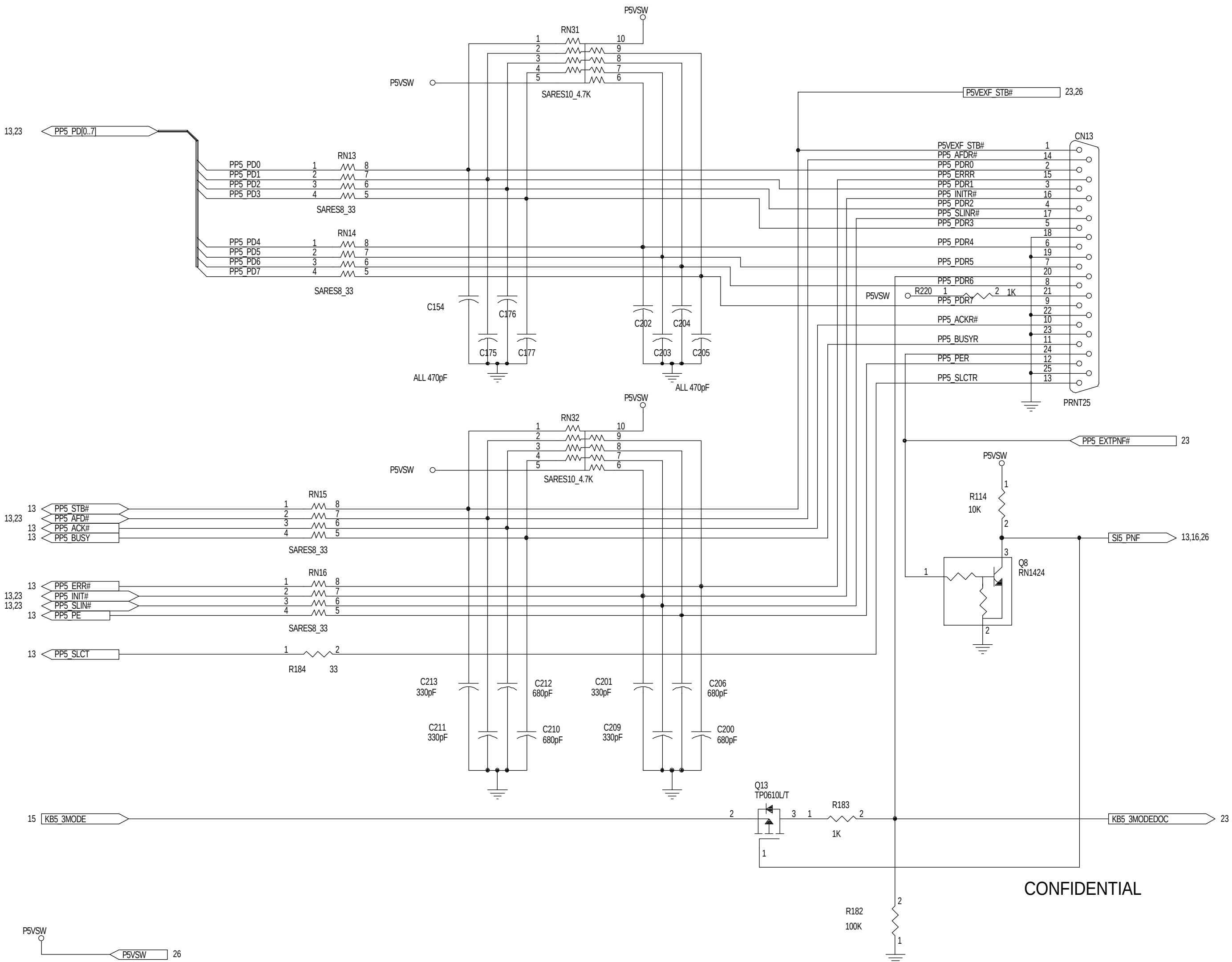
ACER ADVANCED LABS	
Title	PROJECT MARS
Size A3	Document Number: SYSTEM MANAGERMENT CONTROLLER
Date: May 15, 1996	Sheet 16 of 2?



CONFIDENTIAL

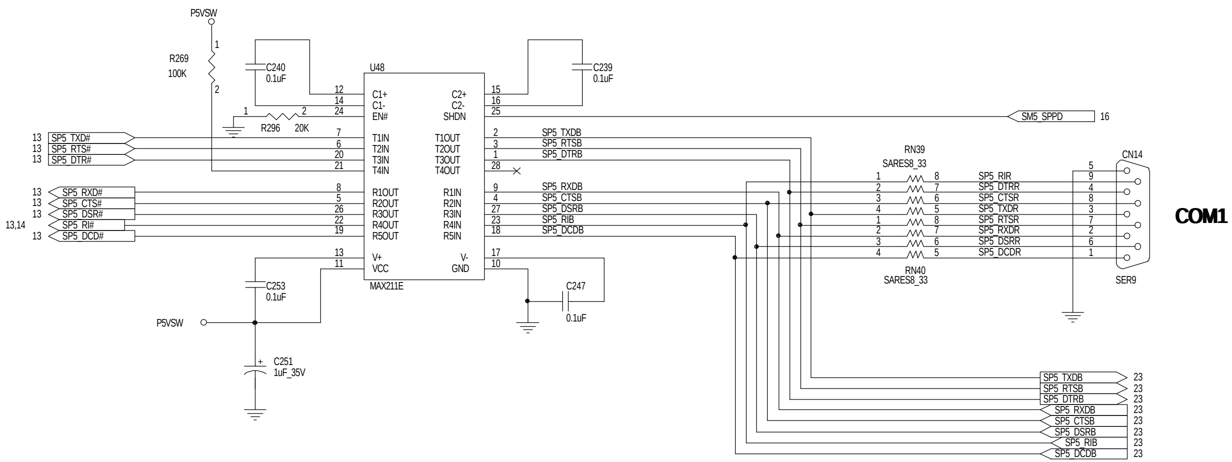
ACER ADVANCED LABS	
Title	PROJECT MARS
Size A3	Document Number: HDD AND CD/FDD INTERFACE
Date: June 6, 1996	Sheet 17 of 33

In order to minimize the crosstalk in ECP mode,
the termination circuits shown below are recommended
Place all termination circuits close to the connector to avoid EMI

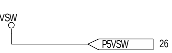


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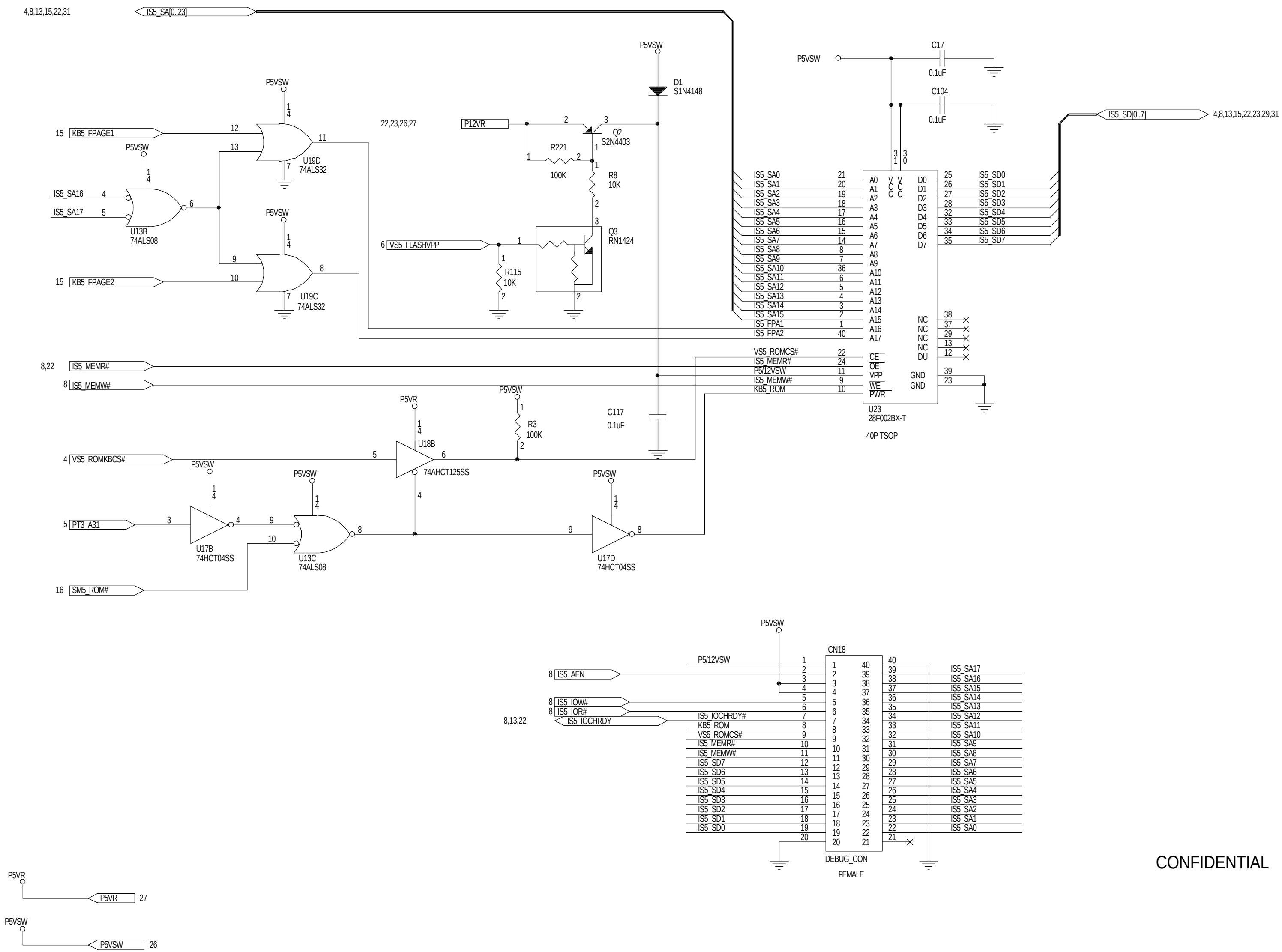
ACER ADVANCED LABS		
Title	PROJECT MARS	
Size A3	Document Number PARALLEL PORT INTERFACE	
Date: May 8, 1996	Sheet 18	of 33



CONFIDENTIAL

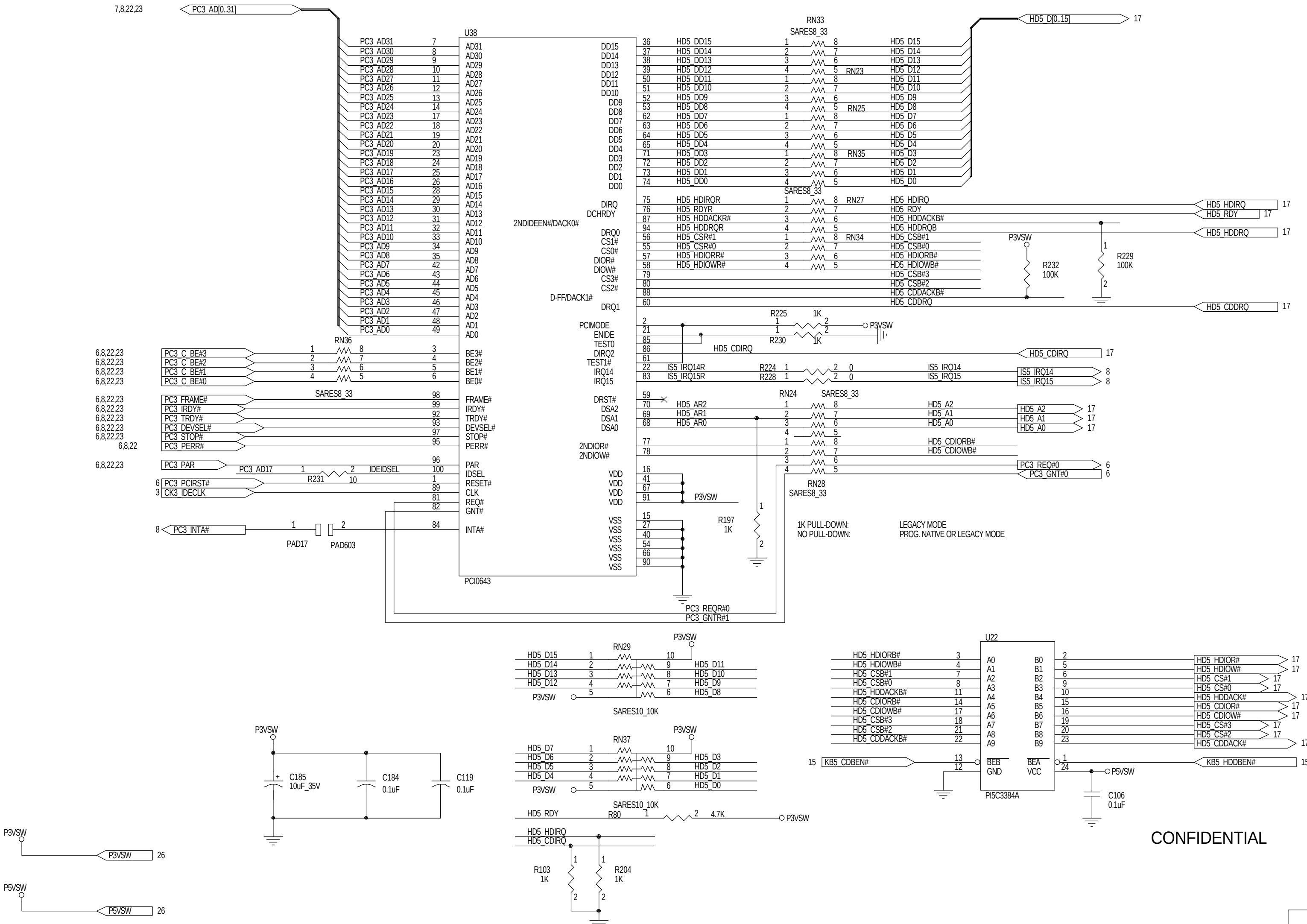


ACER ADVANCED LABS			
Title: PROJECT MARS			
Size: A3	Document Number: SERIAL PORT INTERFACE		REV: 3.0
Date: May 9, 1996	Sheet 19 of 33		



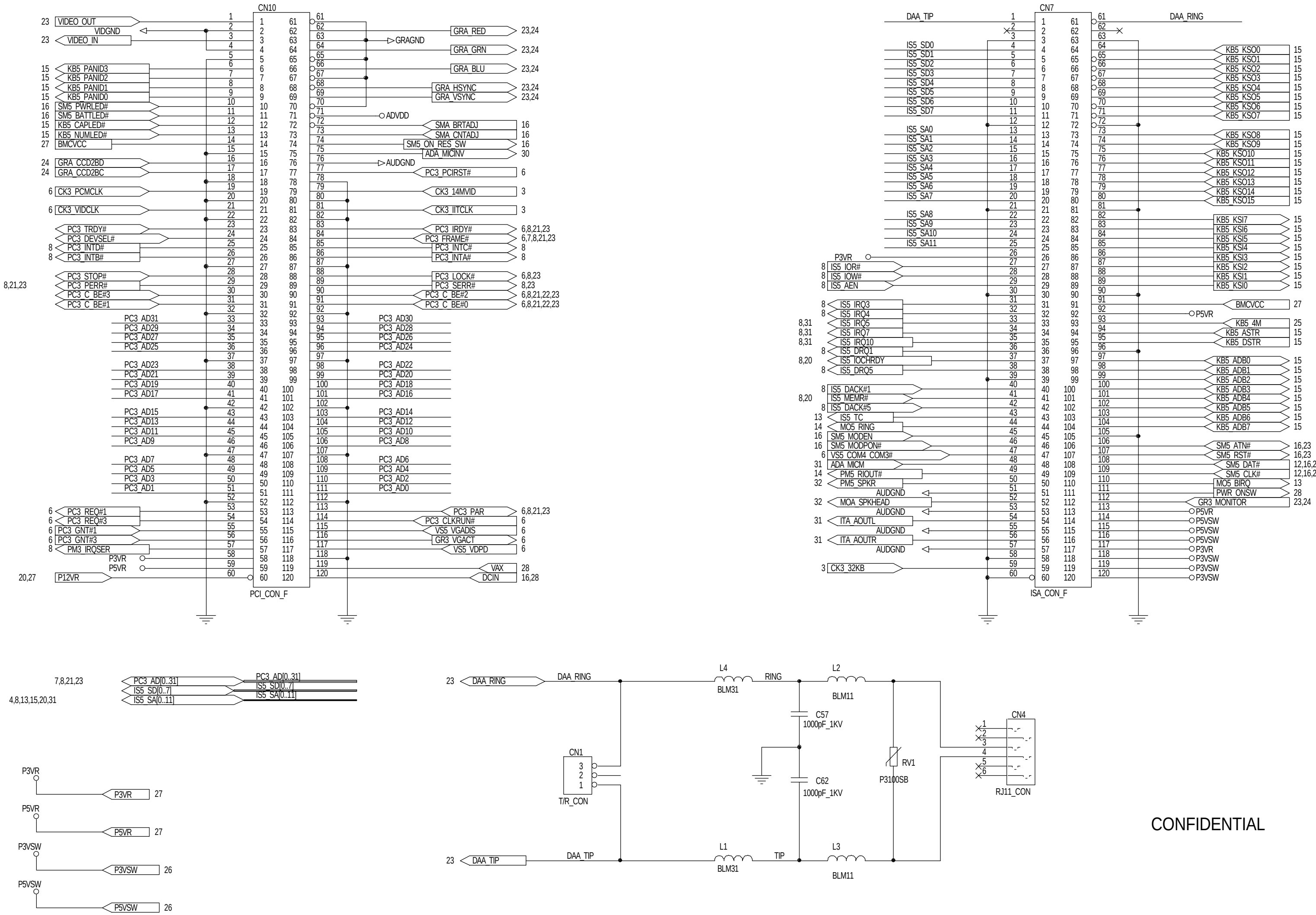
CONFIDENTIAL

ACER ADVANCED LABS	
Title	PROJECT MARS
Size A3	Document Number FLASH BIOS
Date: June 5, 1996	Sheet 20 of



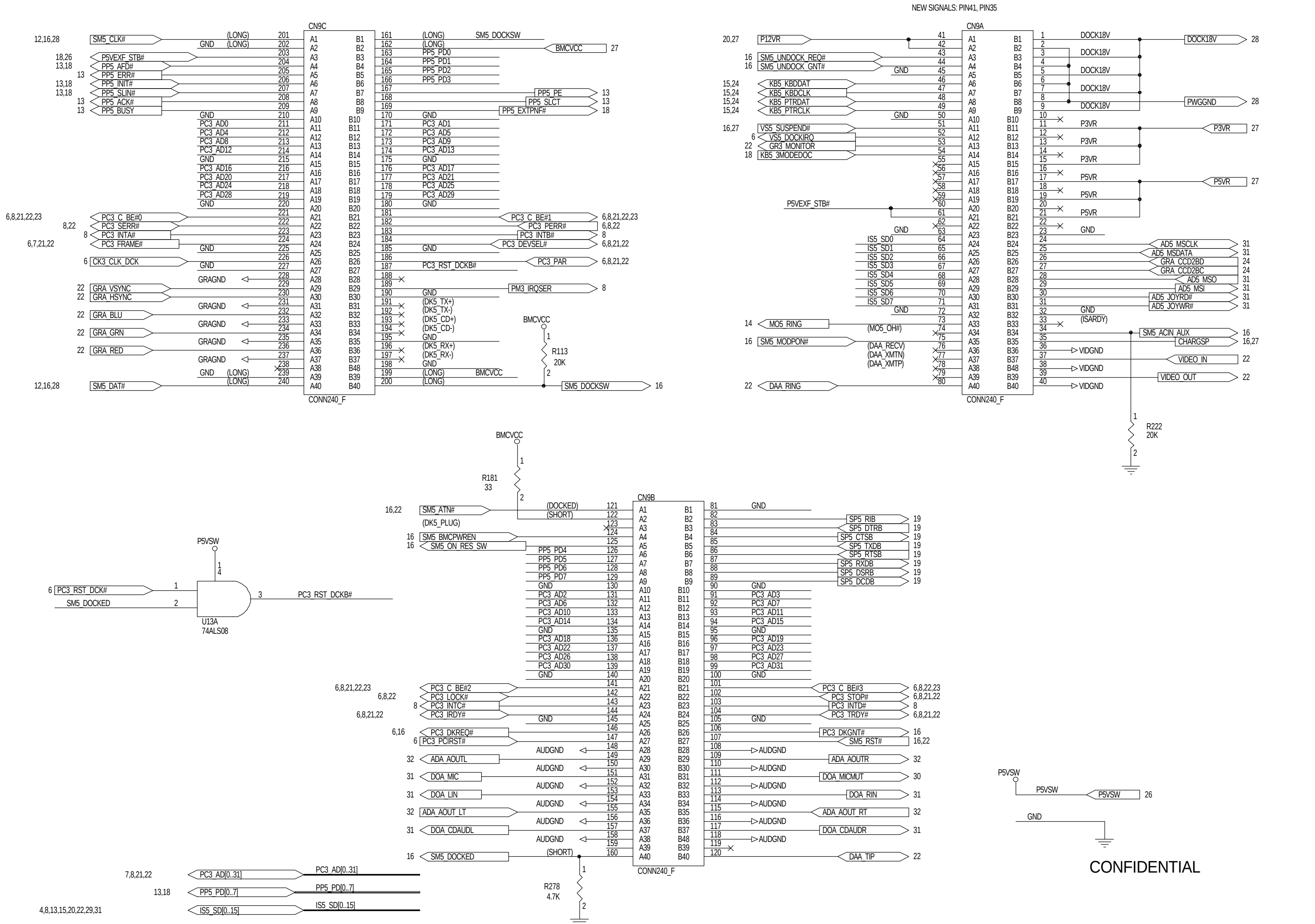
CONFIDENTIAL

ACER ADVANCED LABS				
Title	MARS MAIN BOARD			
Size	Document Number			
A3	BUS MASTER IDE CONTROLLER			
Date:	May 15, 1996	Sheet	21	of 33

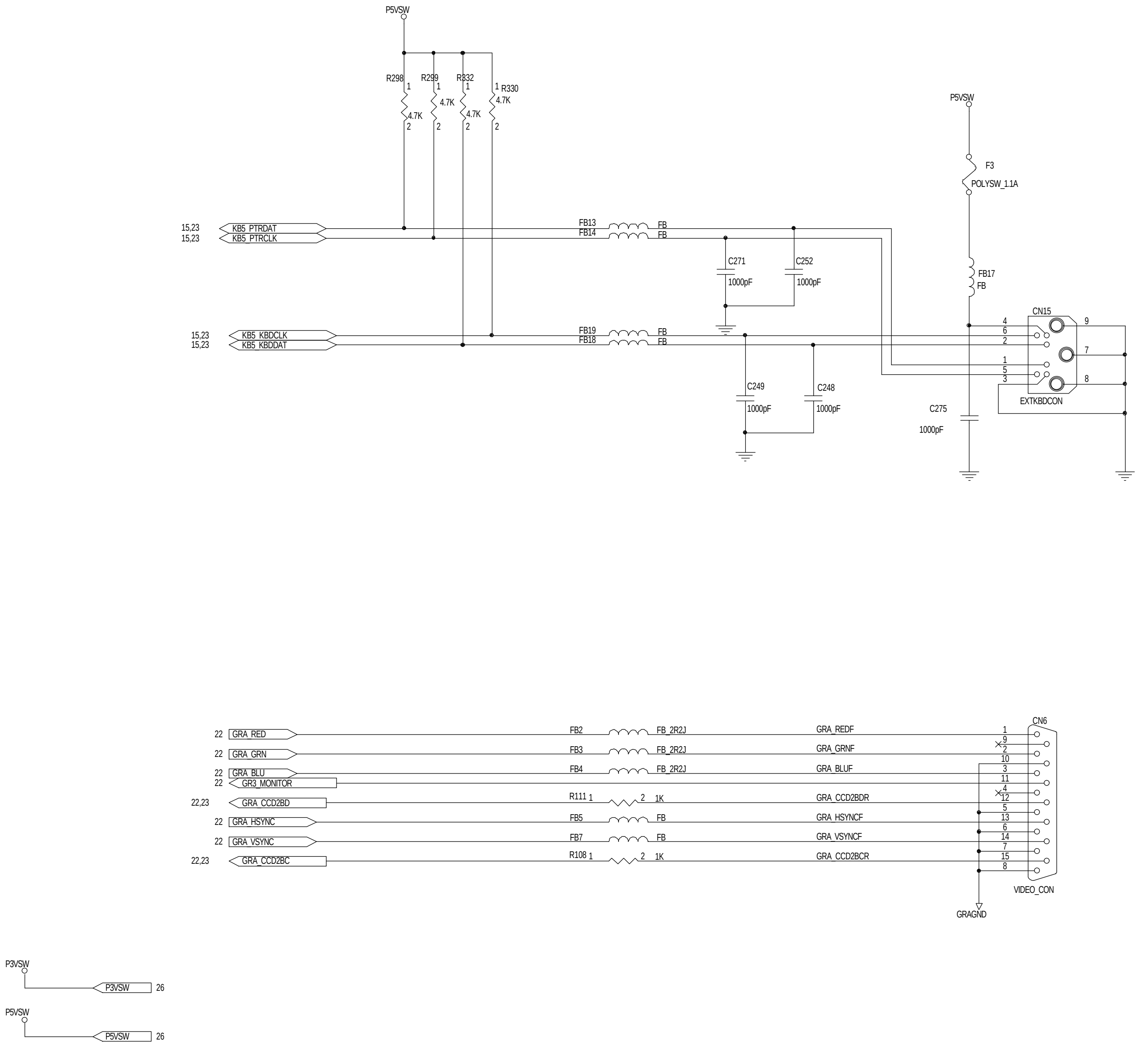


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ACER ADVANCED LABS	
Title	PROJECT MARS
Size A3	Document Number MULTI-MEDIA BOARD CONNECTOR
Date: June 6, 1996	Sheet 22 of

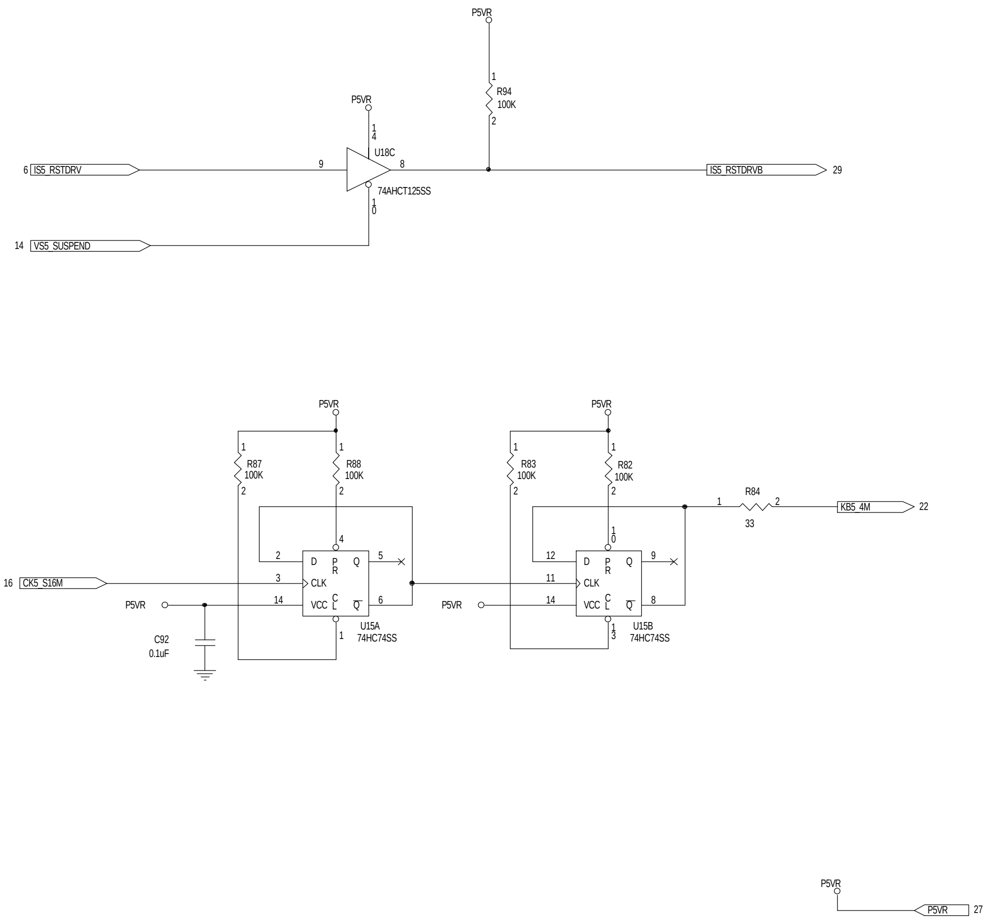


ACER ADVANCED LABS	
Title	PROJECT MARS
Size A3	Document Number: DOCKING CONNECTOR
Date: May 8, 1996	Sheet 23 of



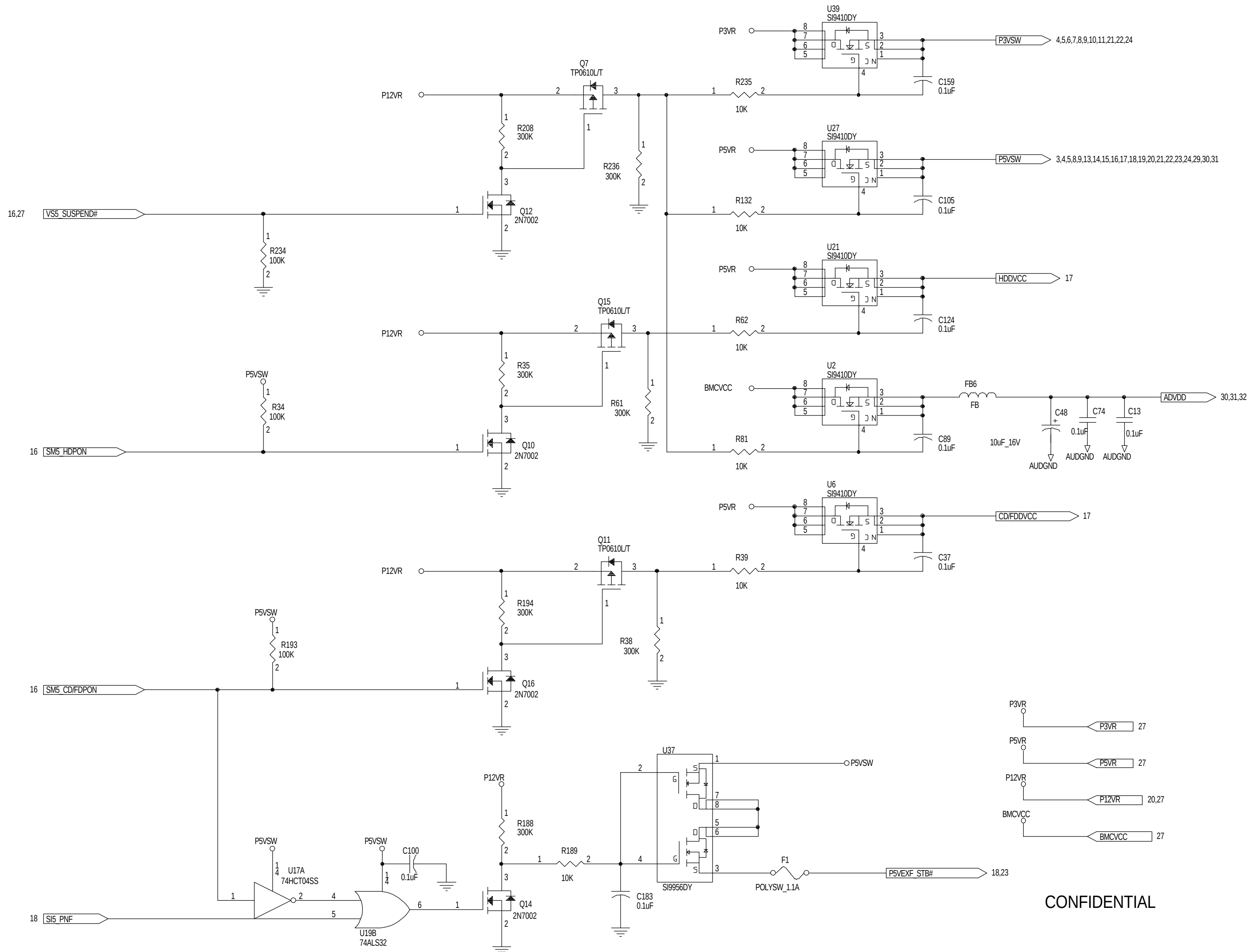
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ACER ADVANCED LABS	
Title	PROJECT MARS
Size A3	Document Number CONNECTOR FOR KEYBOARD MASTER
Date: June 5, 1996	Sheet 24 of 33

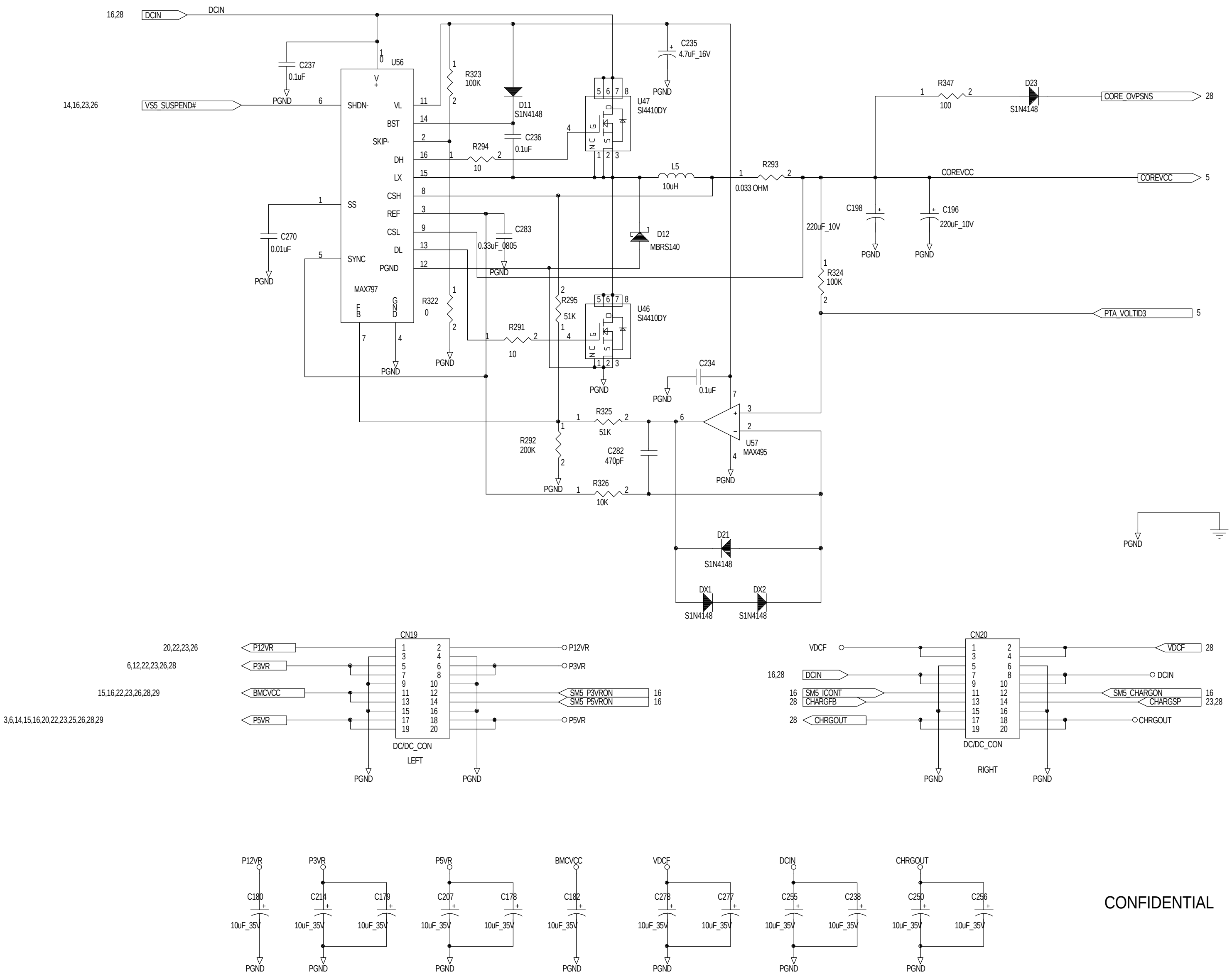


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ACER ADVANCED LABS	
Title	PROJECT MARS
Size A3	Document Number ISOLATION CIRCUITS

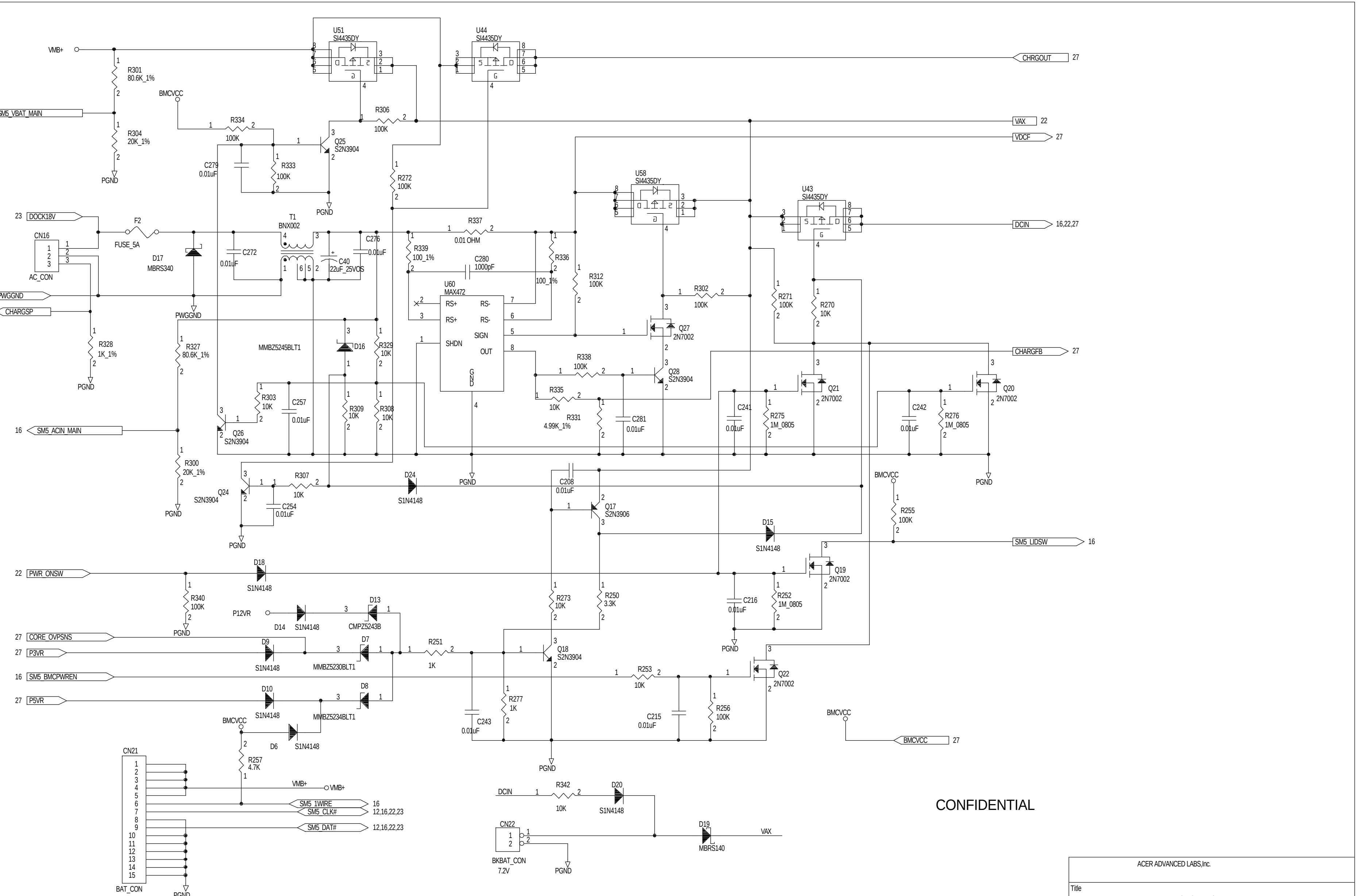


ACER ADVANCED LABS				
Title	PROJECT MARS			
Size A3	Document Number POWER MONITOR			
Date:	May 13, 1996	Sheet	26	of 33



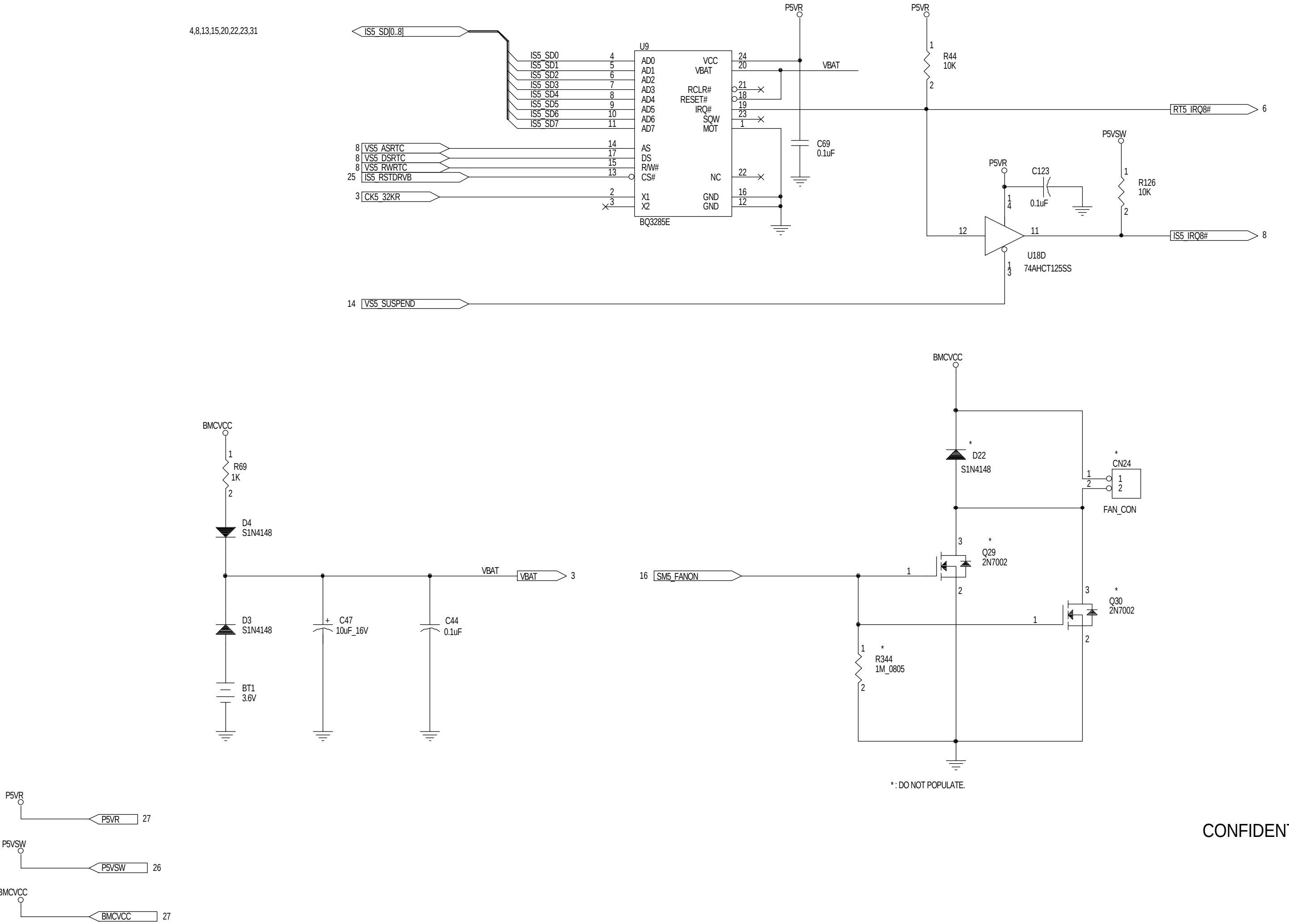
CONFIDENTIAL

ACER ADVANCED LABS	
Title	PROJECT MARS
Size A3	Document Number DC/DC CONVERTER



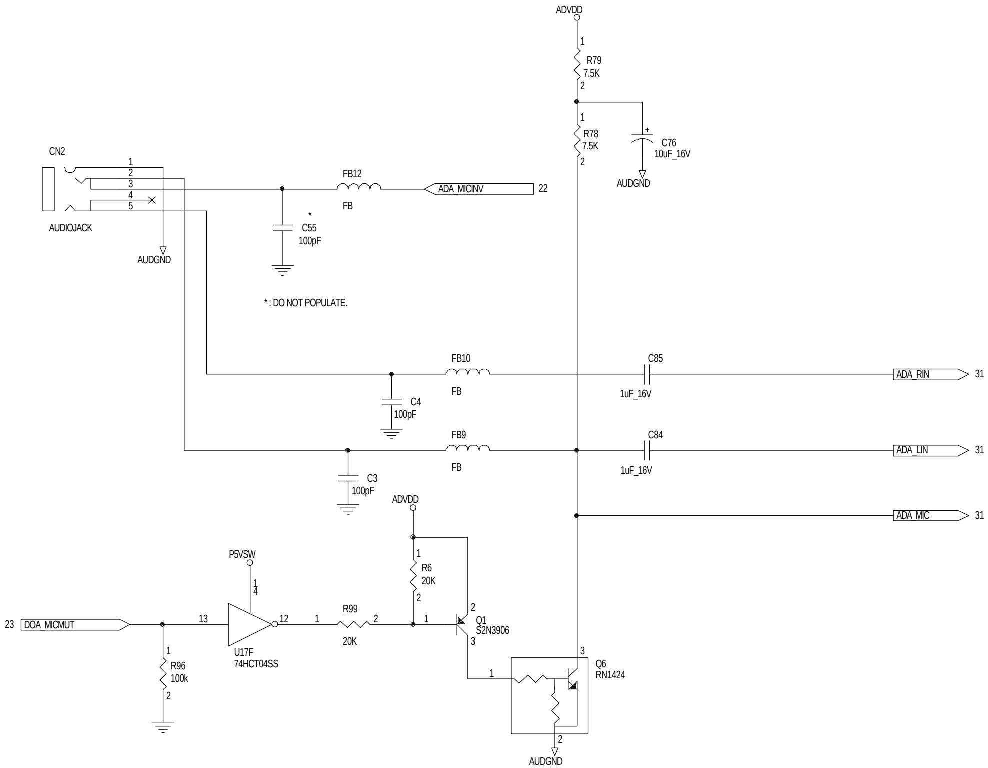
CONFIDENTIAL

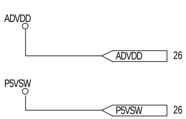
ACER ADVANCED LABS,Inc.		
Title	PROJECT MARS	
Size A3	Document Number POWER ROUTING	REV 3.0
Date: May 9, 1996	Sheet 28 of 32	



CONFIDENTIAL

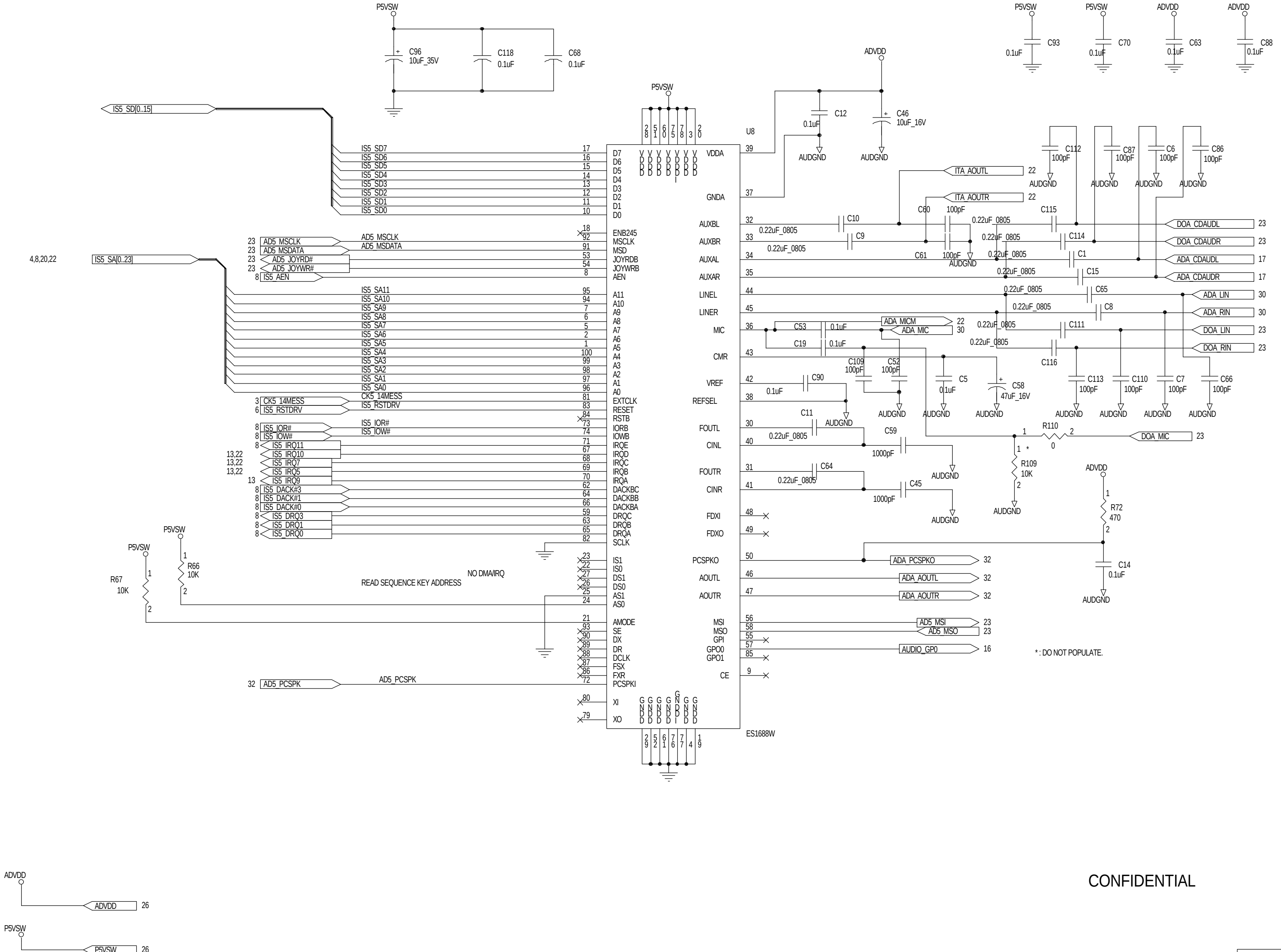
ACER ADVANCED LABS		
Title	PROJECT MARS	
Size A3	Document Number	RTC BATTERY
Date:	May 8, 1996	Sheet 20 of





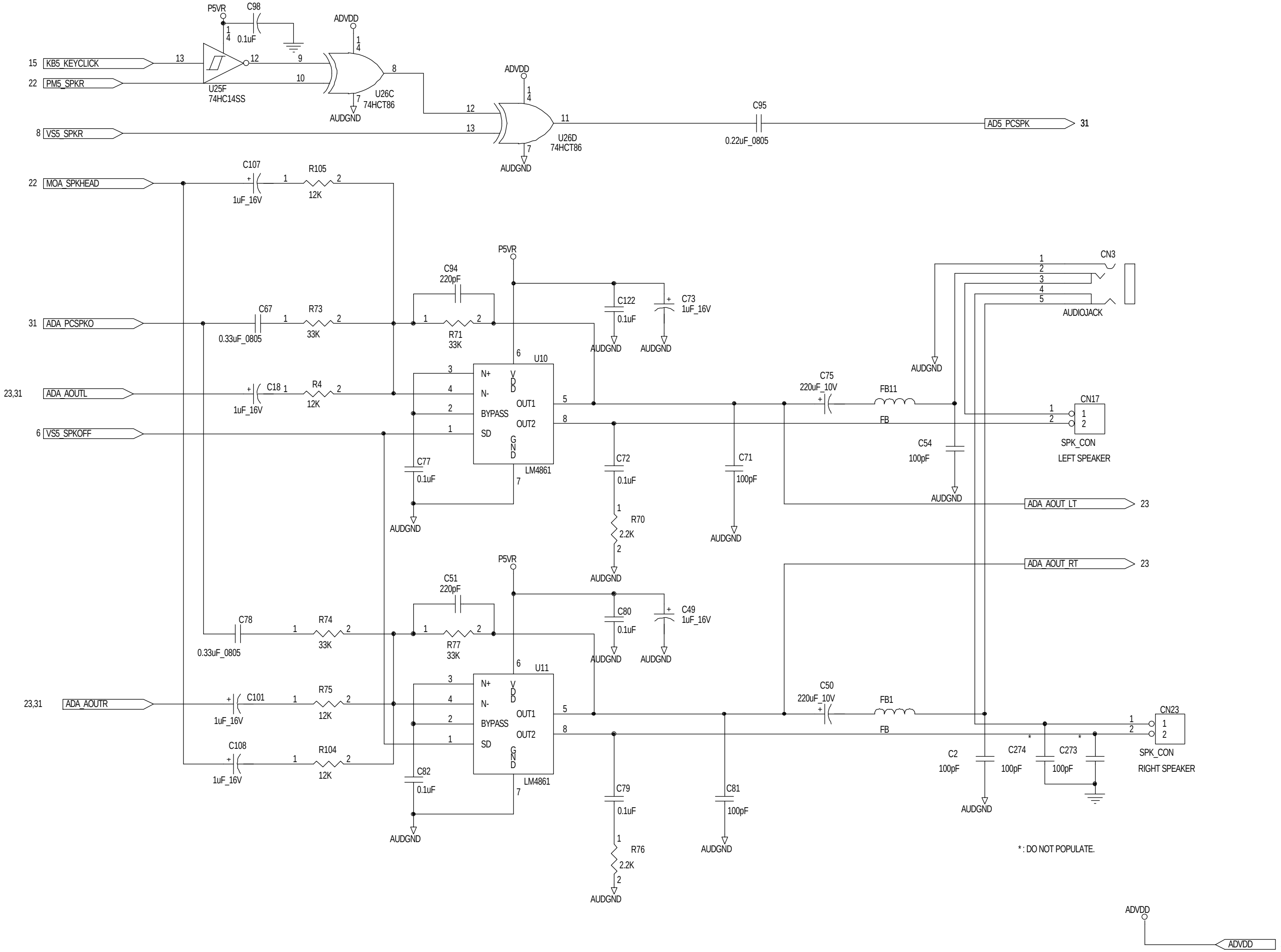
CONFIDENTIAL

ACER ADVANCED LABS				
Title: PROJECT MARS				
Size: A3	Document Number: MIC INPUT CIRCUIT			
Date: June 11, 1996		Sheet 30	of	3



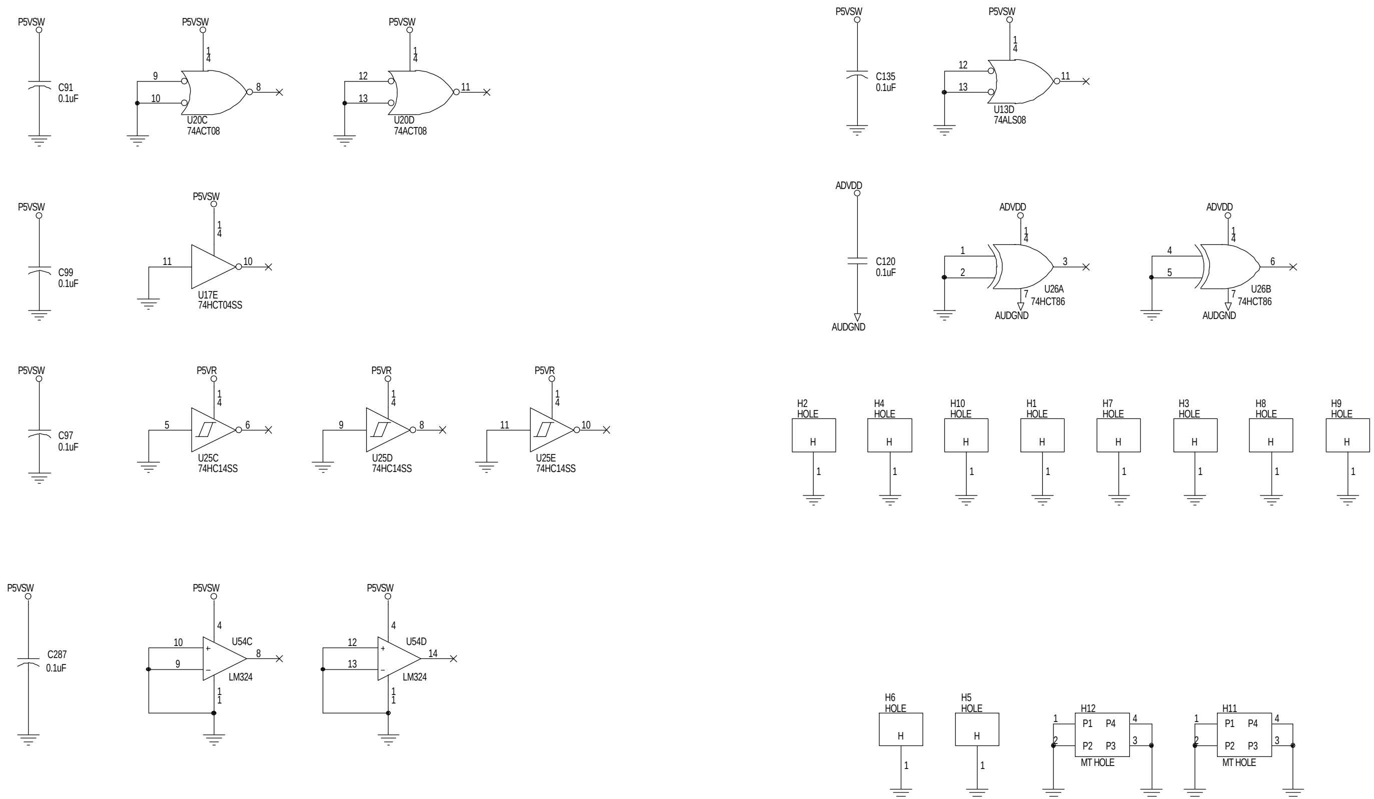
CONFIDENTIAL

ACER ADVANCED LABS		
Title	PROJECT MARS	
Size A3	Document Number	AUDIO CODEC
Date: June 11, 1996	Sheet 31	of 3



CONFIDENTIAL

ACER ADVANCED LABS	
Title	PROJECT MARS
Size A3	Document Number SPEAKER OUTPUT CIRCUIT
Date: June 11, 1996	Sheet 22 of 2[illegible]



CONFIDENTIAL

ACER ADVANCED LABS	
Title	PROJECT MARS
Size A3	Document Number SPARE PARTS
Date: May 15, 1996	Sheet 33 of 33

REVISION HISTORY

I. MODIFICATIONS FROM X4 TO X5

1. DELETE COMPONENTS:

C78: 0.01uF 10% CAP

2. VALAUE CHANGES:

R13: 20K 5% RESISTOR	-->	1K 5% RESISTOR
R50: 10K 5% RESISTOR	-->	4.7K 5% RESISTOR

3. ADD COMPONENTS:

R80,R83: 10K 5% RESISTOR
R81,R82: 15K 5% RESISTOR
R84: 4.7K 5% RESISTOR
R85,R86: 150K 5% RESISTOR
C137: 4700pF 10% CAP
C138: 0.47uF 10% CAP 0805

II. POPULATED/UNPOPULATED PARTS

1. NMG2090 VIDEO CONTROLLER

UNPOPULATED PARTS:	U25 R63,R66,R67,R68,R73,R74,R77,R78,R83 C42,C123,C124,C125,C126 CN1

2. NMG2093 VIDEO CONTROLLER

POPULATED PARTS:	U25 R83 C42,C123,C124,C125,C126
UNPOPULATED PARTS:	R63,R66,R67,R68,R73,R74,R77,R78 CN1

CONFIDENTIAL

ACER ADVANCED LABS.				
Title	PROJECT MARS MULTI-MEDIA BOARD			
Size A3	Document Number REVISION HISTORY			
Date: May 23, 1996	Sheet	2	of	14

Tfhis section shows the **media board** schematic diagrams of the notebook.

<u>*Schematics Page List:*</u>

PROJECT MARS MULTI-MEDIA BOARD

LINK
FMD2.SCH
FMD3.SCH
FMD4.SCH
FMD5.SCH
FMD6.SCH
FMD7.SCH
FMD8.SCH
FMD9.SCH
FMD10.SCH
FMD11.SCH
FMD12.SCH
FMD13.SCH
FMD14.SCH

CONFIDENTIAL

ACER ADVANCED LABS				
Title: PROJECT MARS MULTI-MEDIA BOARD (X5)				
Size: A3	Document Number: MULTI-MEDIA BOARD			
Date: May 1, 1996	Sheet	1	of	14

REVISION HISTORY

I. MODIFICATIONS FROM X4 TO X5

1. DELETE COMPONENTS:

C78: 0.01uF 10% CAP

2. VALAUE CHANGES:

R13: 20K 5% RESISTOR	-->	1K 5% RESISTOR
R50: 10K 5% RESISTOR	-->	4.7K 5% RESISTOR

3. ADD COMPONENTS:

R80,R83: 10K 5% RESISTOR
R81,R82: 15K 5% RESISTOR
R84: 4.7K 5% RESISTOR
R85,R86: 150K 5% RESISTOR
C137: 4700pF 10% CAP
C138: 0.47uF 10% CAP 0805

II. POPULATED/UNPOPULATED PARTS

1. NMG2090 VIDEO CONTROLLER

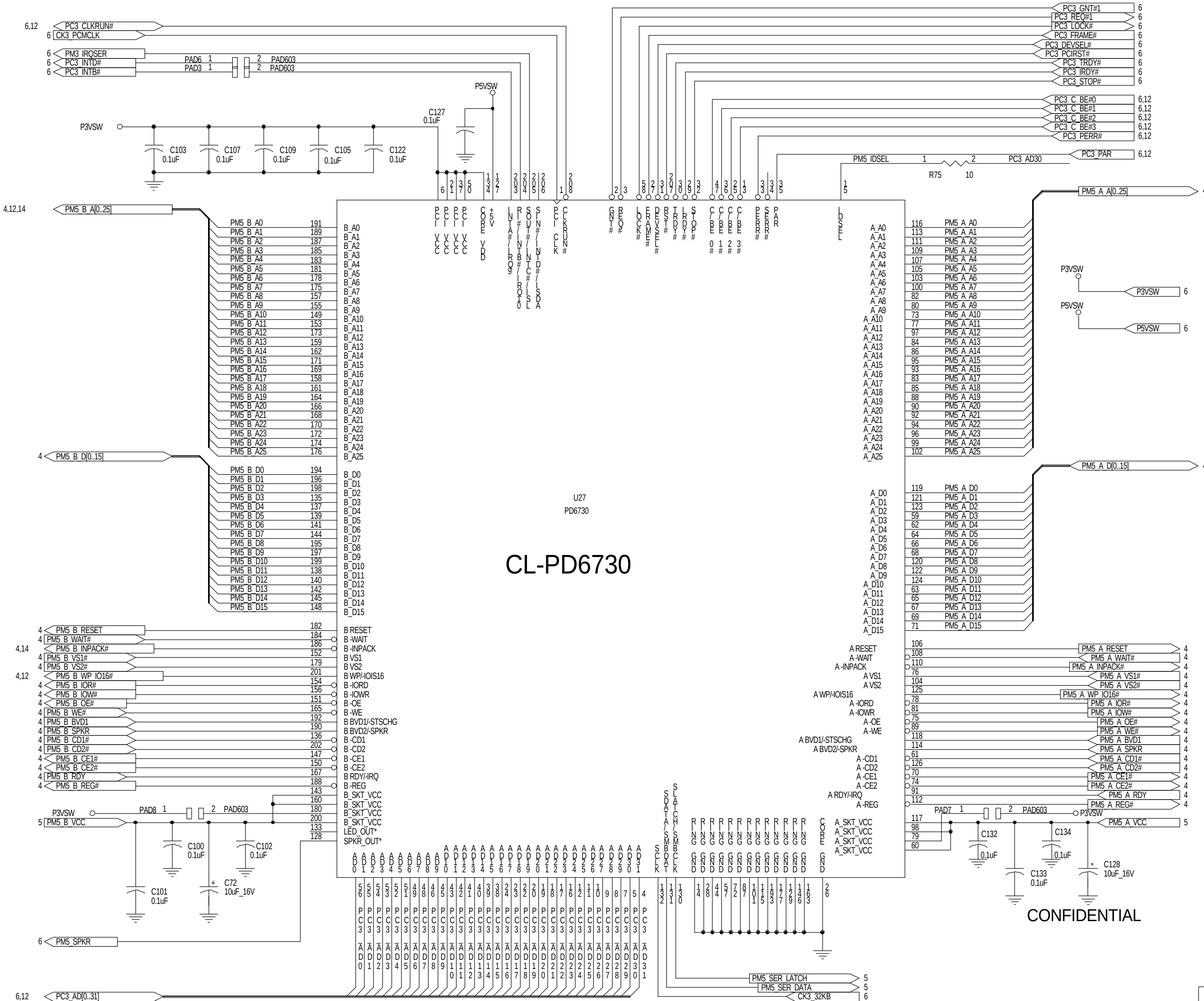
UNPOPULATED PARTS:	U25 R63,R66,R67,R68,R73,R74,R77,R78,R83 C42,C123,C124,C125,C126 CN1

2. NMG2093 VIDEO CONTROLLER

POPULATED PARTS:	U25 R83 C42,C123,C124,C125,C126
UNPOPULATED PARTS:	R63,R66,R67,R68,R73,R74,R77,R78 CN1

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ACER ADVANCED LABS.				
Title	PROJECT MARS MULTI-MEDIA BOARD			
Size: A3	Document Number: REVISION HISTORY			
Date:	May 23, 1996	Sheet	2	of 14

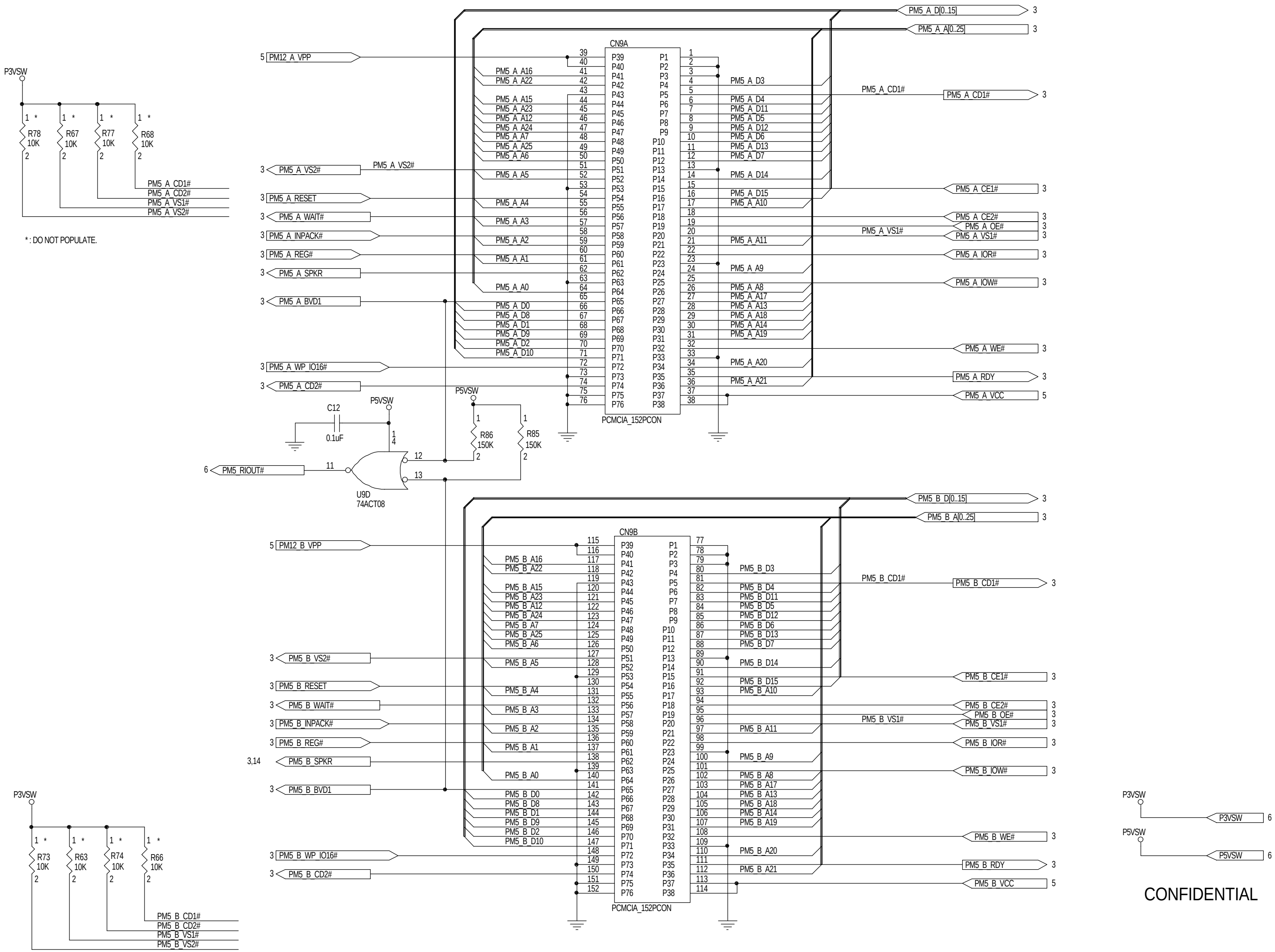


ACER ADVANCED LABS

Title: PROJECT MARS MULTI-MEDIA

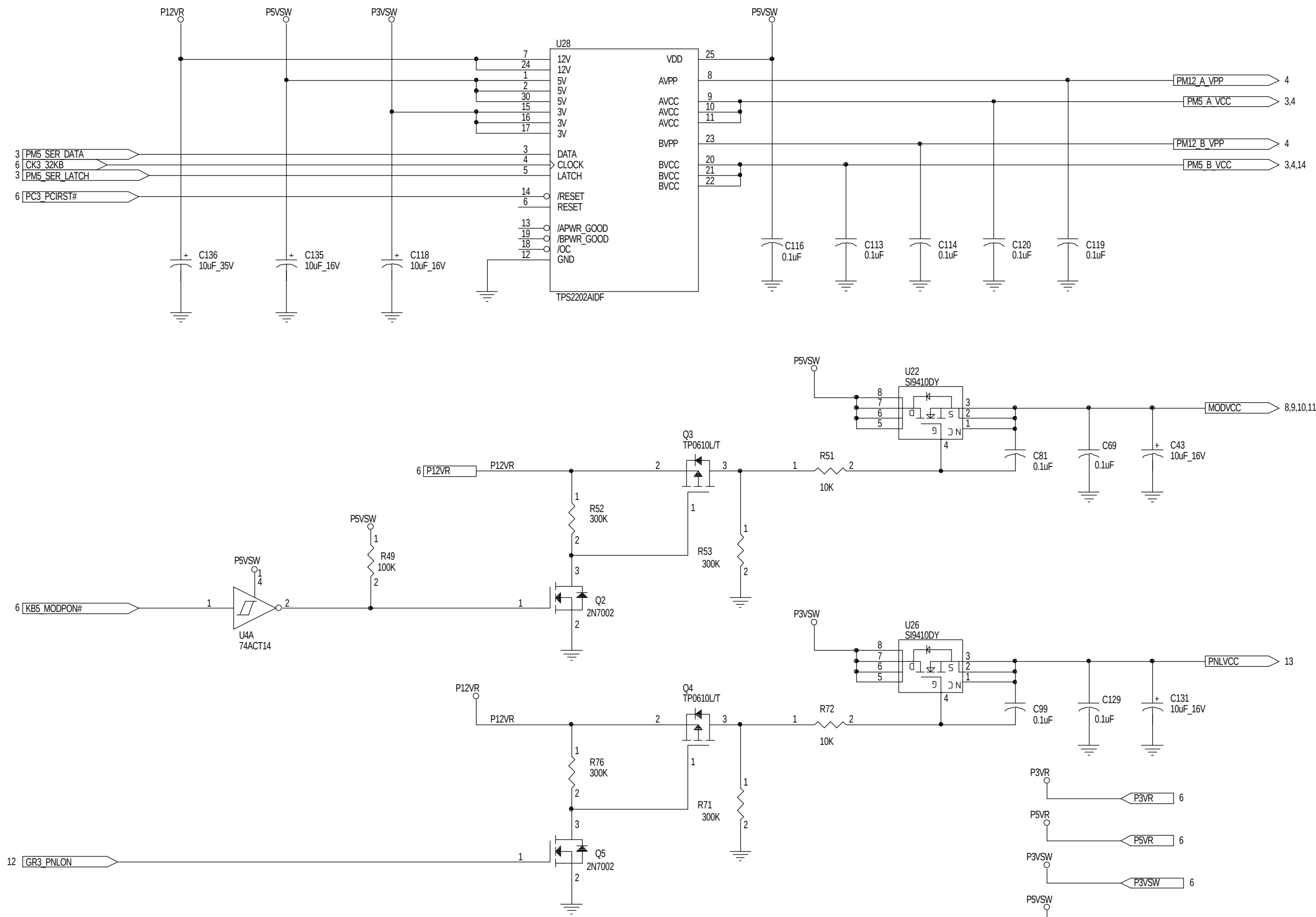
Size: A3 | Document Number: PCMCIA CONTROLLER

Date: May 15, 1996 | Sheet 3 of 14



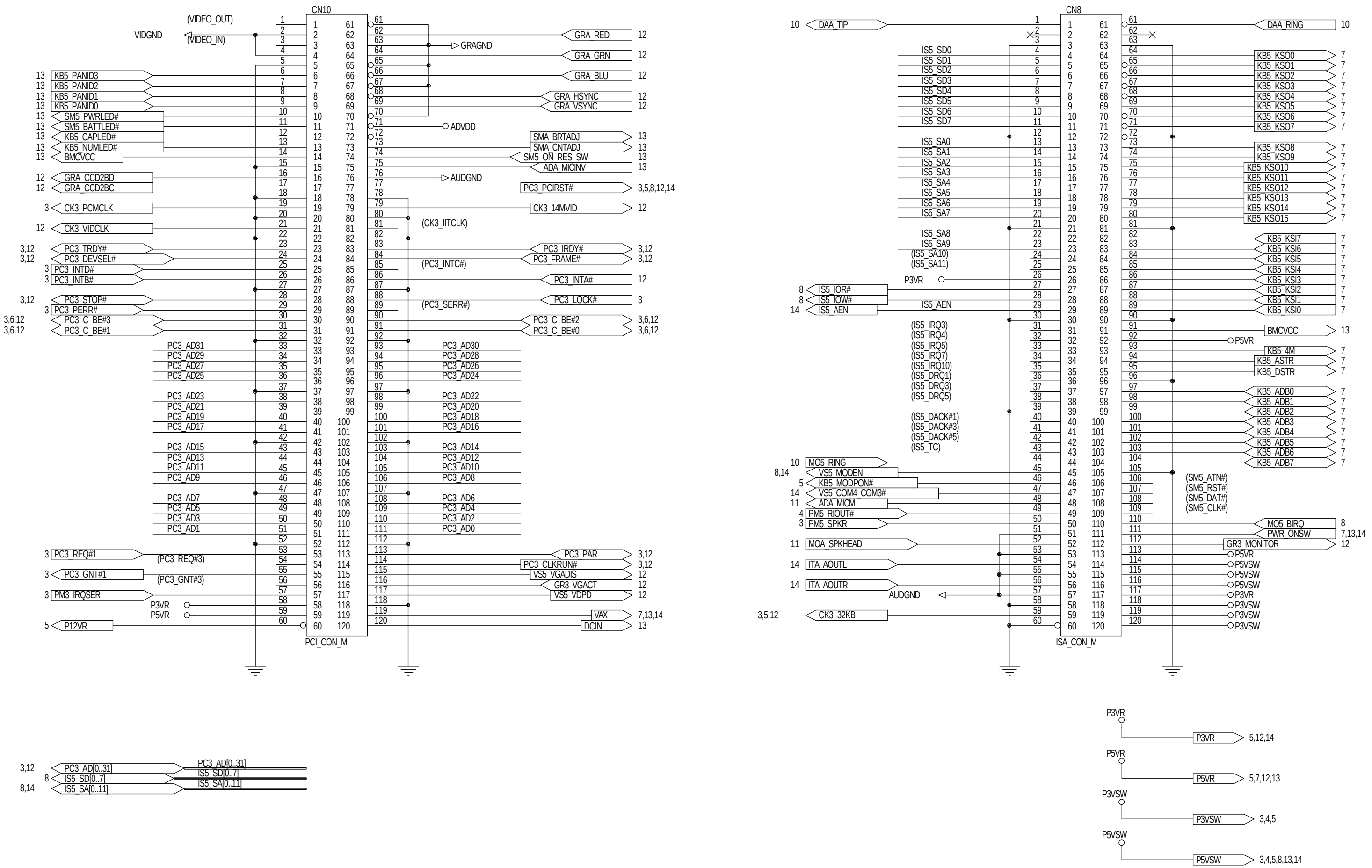
ACER ADVANCED LABS			
Title	PROJECT MARS MULTI-MEDIA		
Size A3	Document Number PCMCIA SOCKETS		
Date: May 23, 1996	Sheet 4	of	1

Note: SW to turn off P12VR during 5V suspend



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ACER ADVANCED LABS				
Title: PROJECT MARS MULTI-MEDIA				
Size: A3	Document Number: PCMCIA SOCKET PWR & INT CONTROL			
Date: May 9, 1996		Sheet	5	of 1



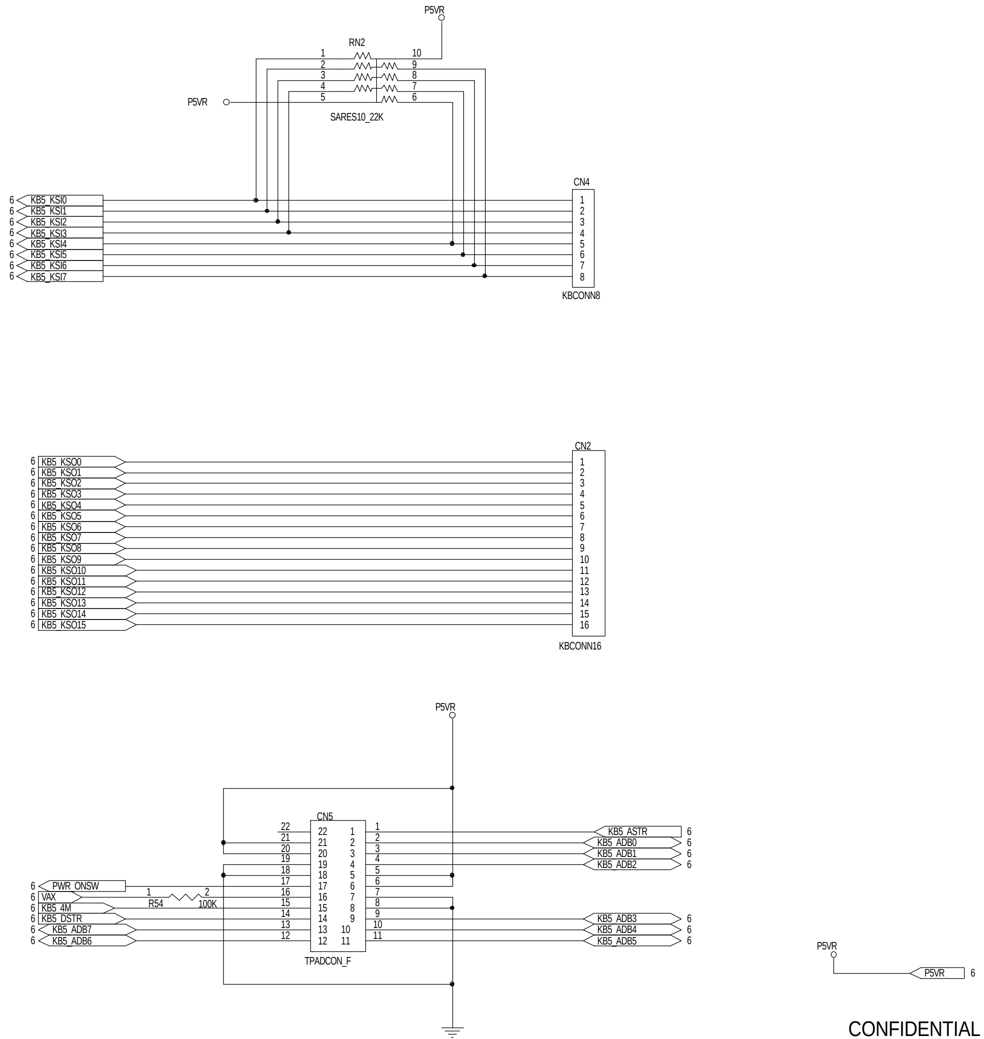
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ACER ADVANCED LABS

Title
PROJECT MARS MULTI-MEDIA

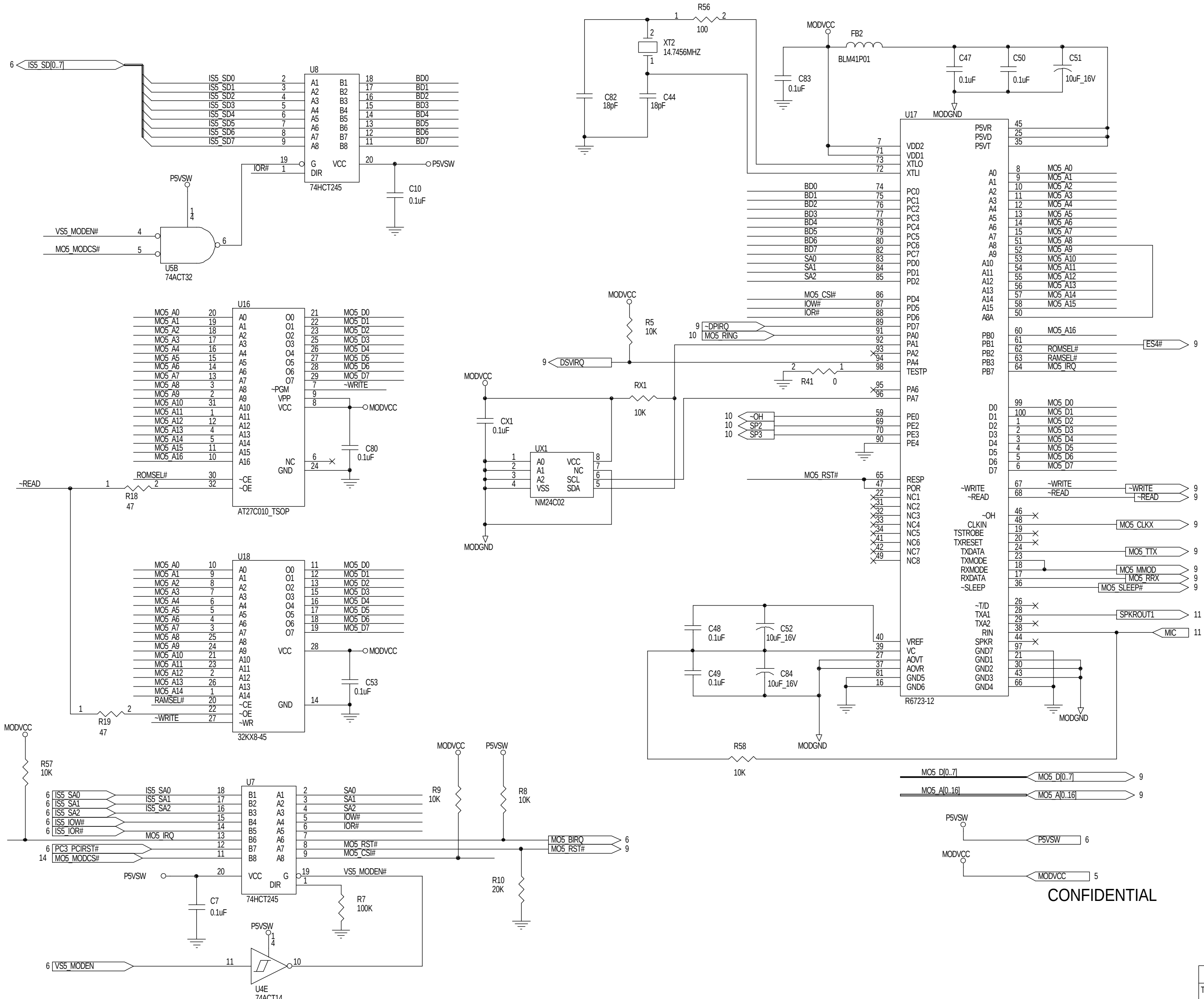
Size A3
Document Number SYSTEM/MEDIA BOARD CONNECTOR

Date: May 15, 1996 Sheet 6 of 14



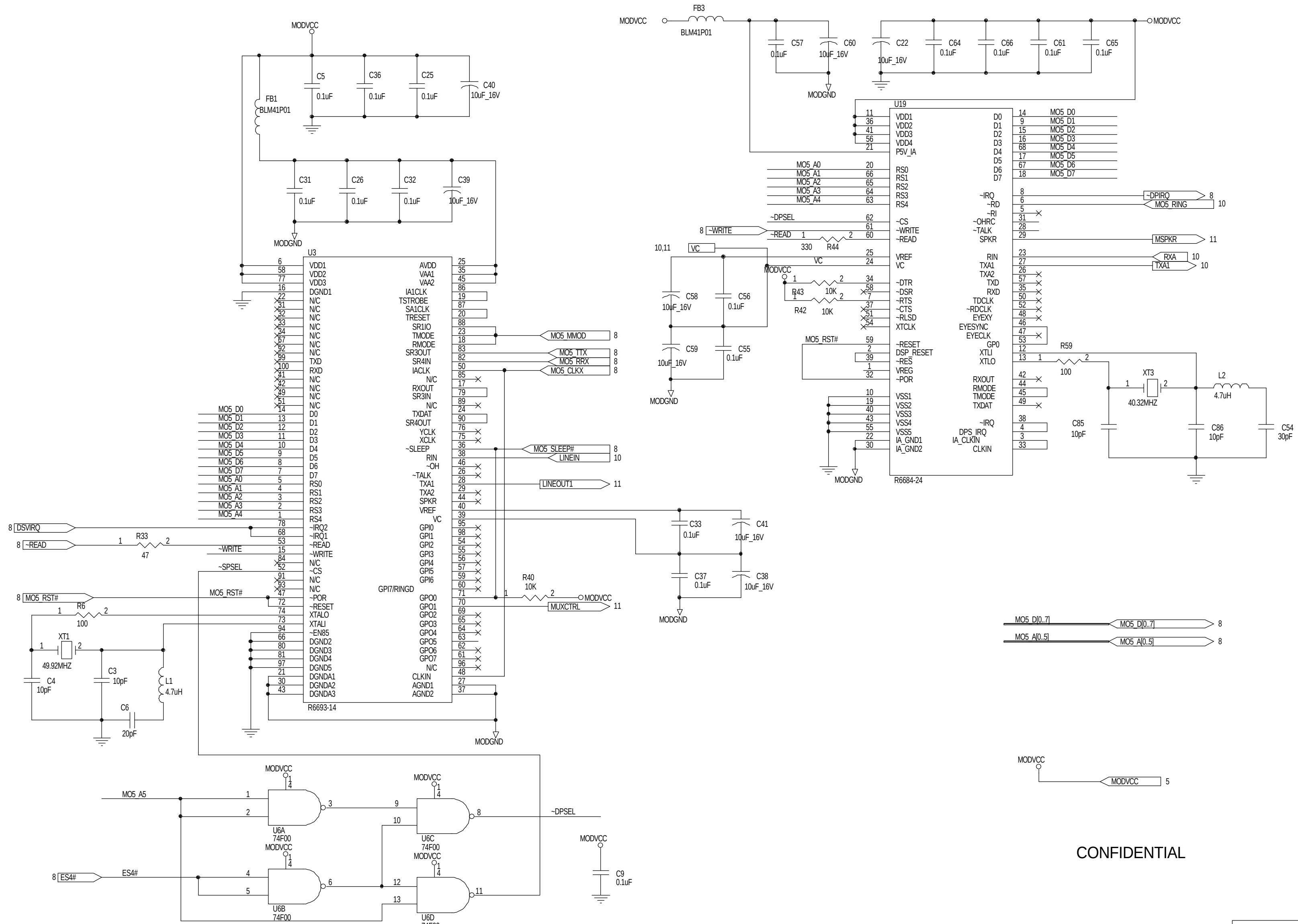
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ACER ADVANCED LABS			
Title: PROJECT MARS MULTI-MEDIA			
Size: A3	Document Number: INTERNAL KBD AND TOUCH PAD CONNECTOR		
Date: May 9, 1996		Sheet 7	of 14



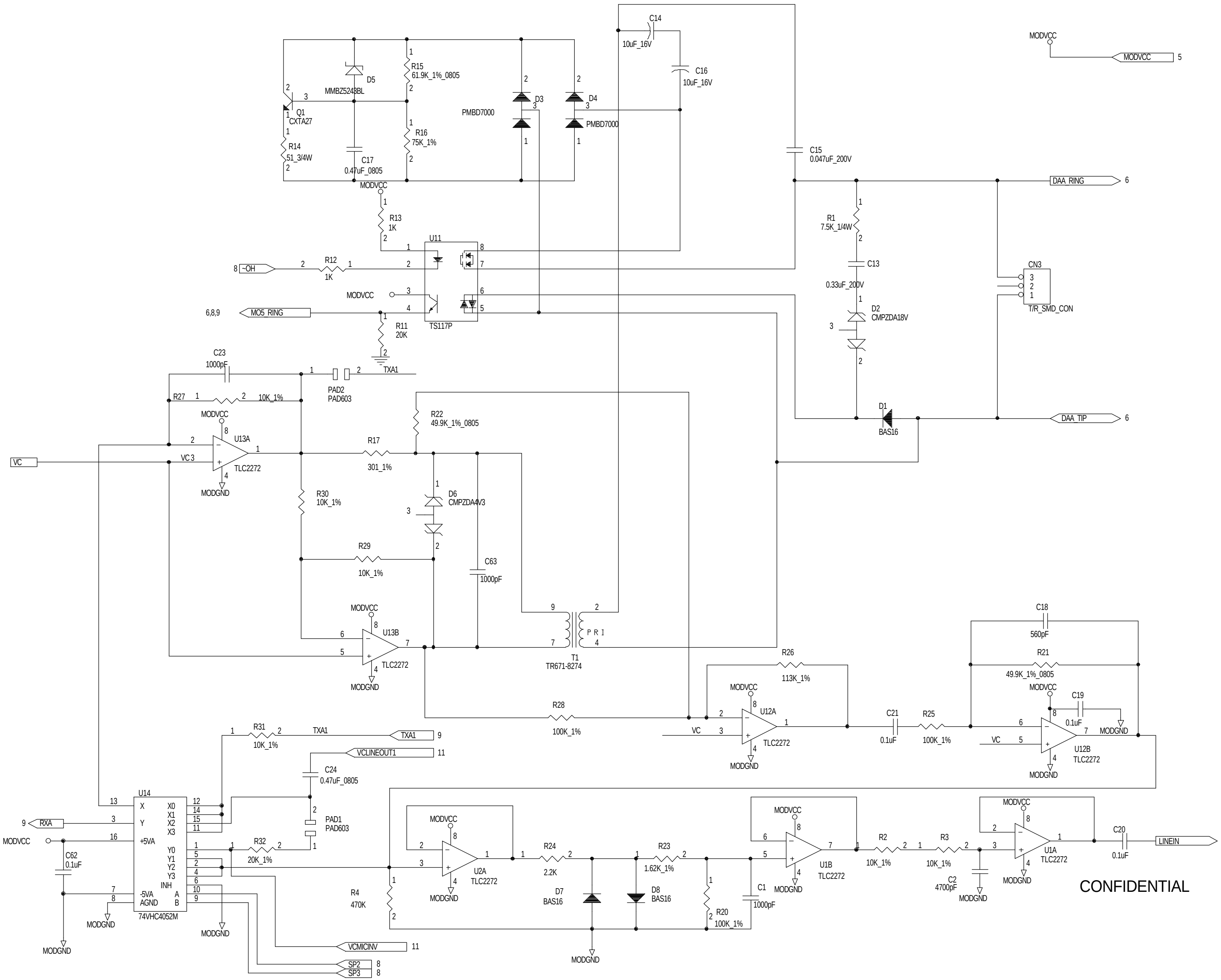
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ACER ADVANCED LABS	
Title	PROJECT MARS MULTI-MEDIA
Size A3	Document Number: PCBUS INTERFACE
Date: June 6, 1996	Sheet 8 of 14



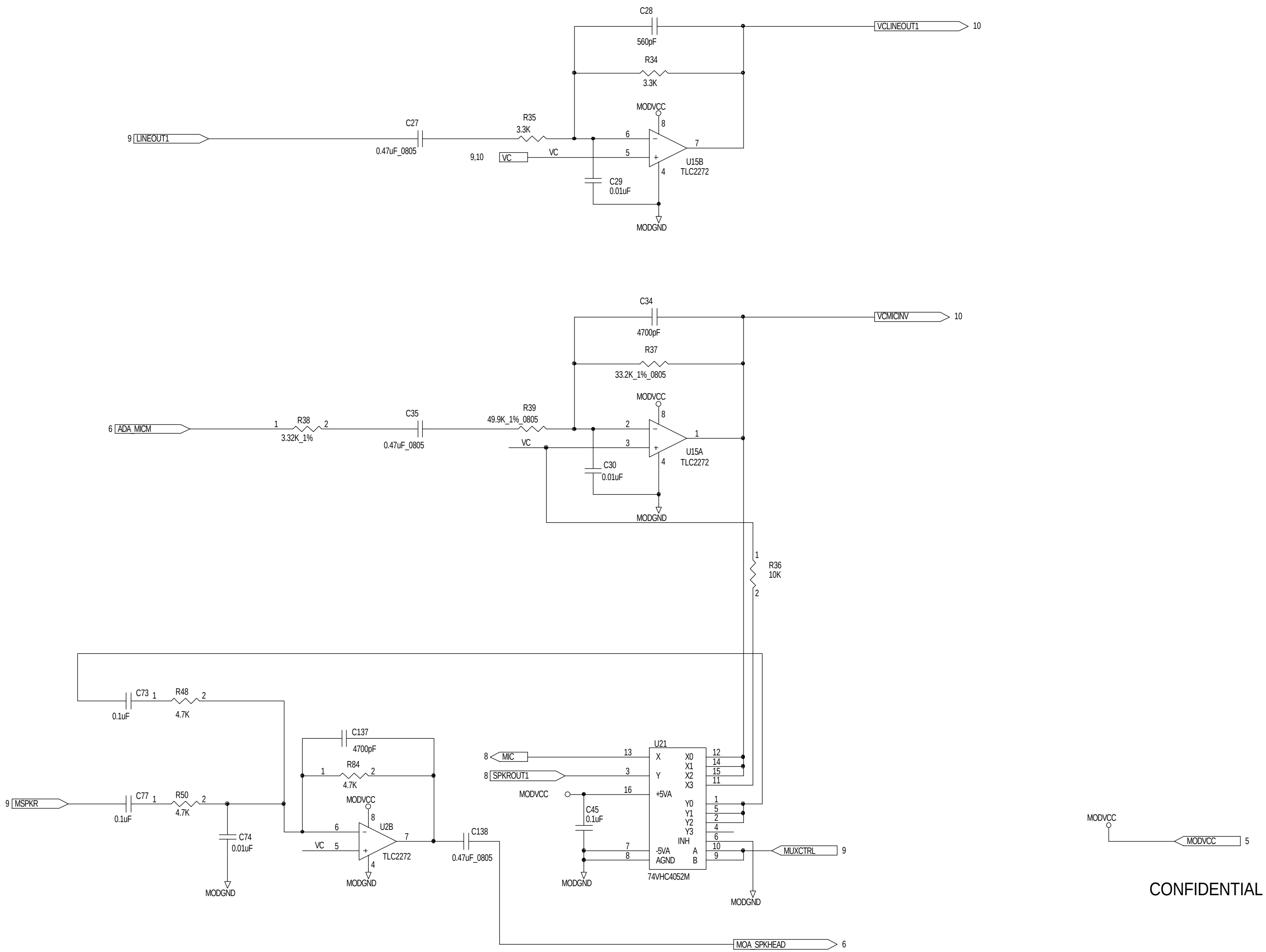
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ACER ADVANCED LABS		
Title	PROJECT MARS MULTI-MEDIA	
Size A3	Document Number DSP INTERFACE	
Date: May 9, 1996	Sheet 9	of 1



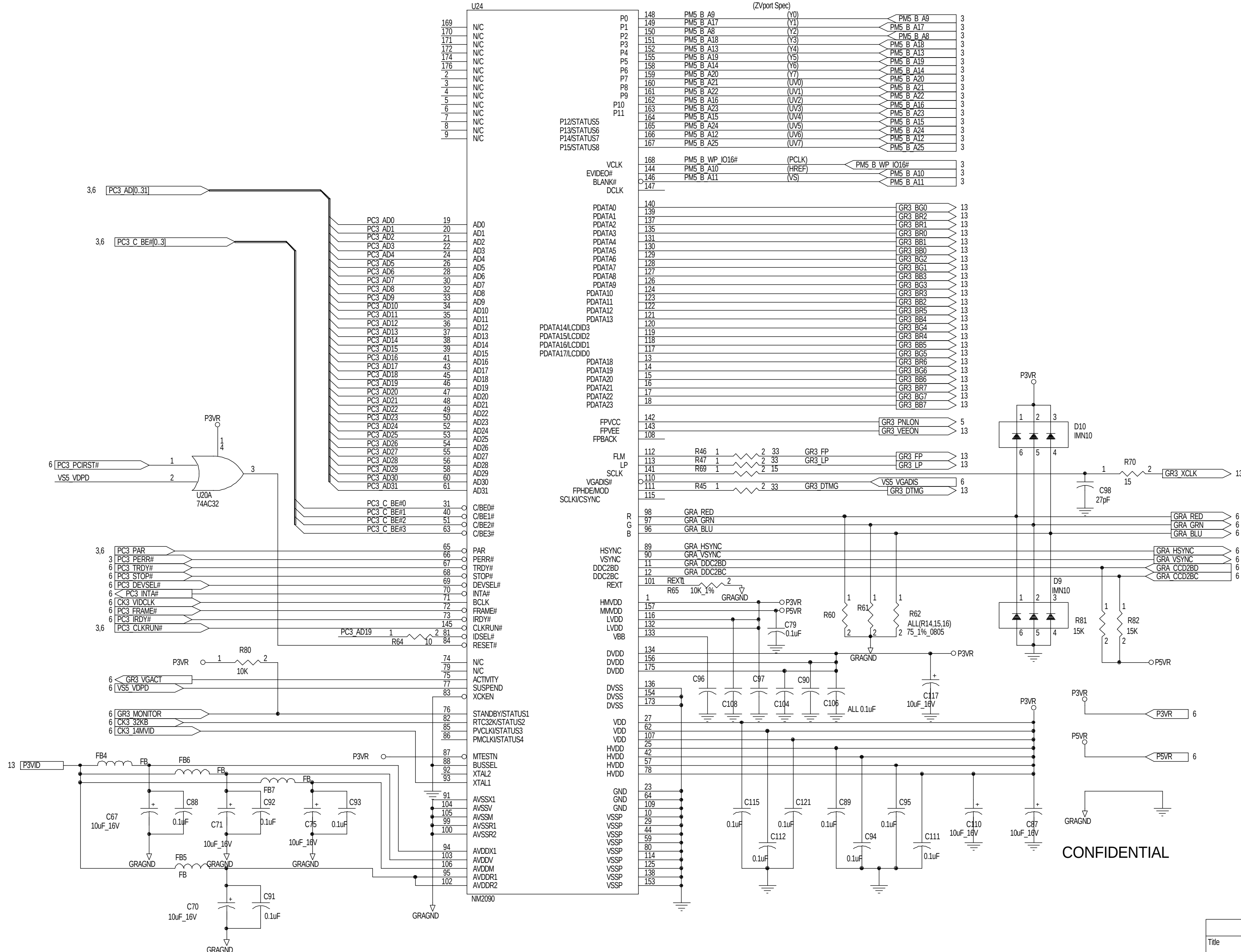
CONFIDENTIAL

	ACER ADVANCED LABS
Title	PROJECT MARS MULTI-MEDIA
Size A3	Document Number PARALLEL DAA
Date: May 23, 1996	Sheet 10 of 14



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ACER ADVANCED LABS			
Title: PROJECT MARS MULTI-MEDIA			
Size: A3	Document Number: DSVD		
Date: May 23, 1996	Sheet	11	of 1[illegible]

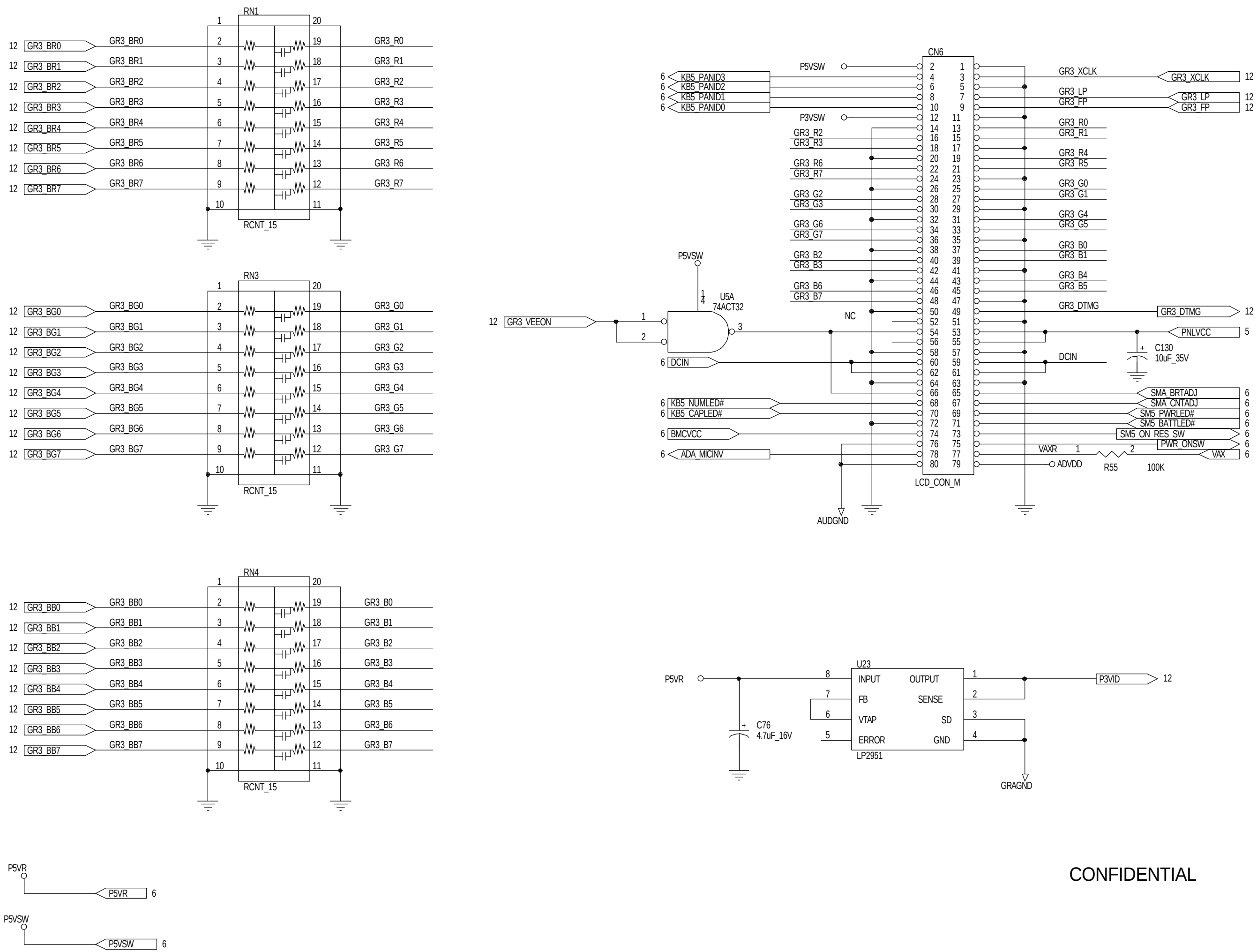


ACER ADVANCED LABS

Title

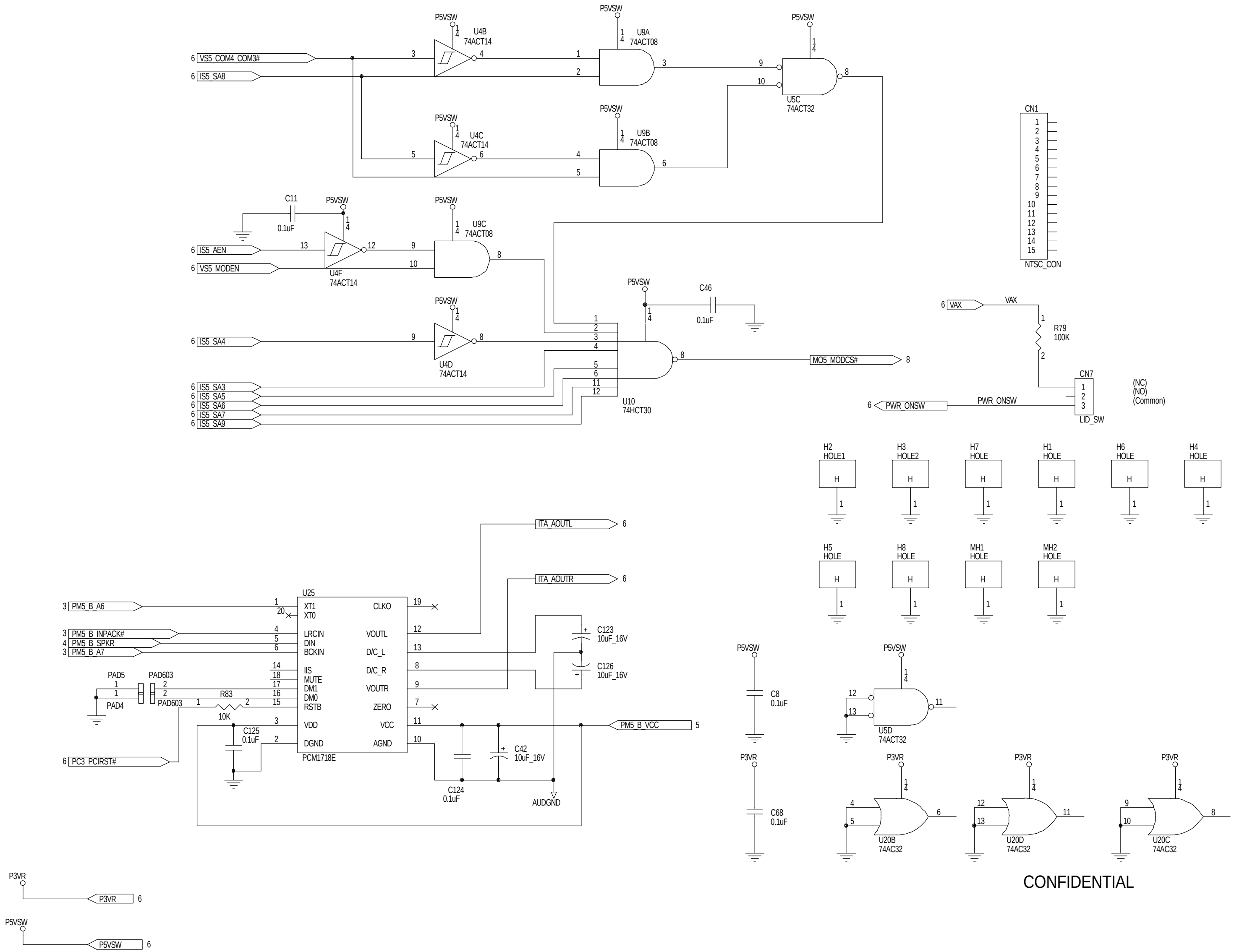
PROJECT MARS MULTI-MEDIA

Size	Document Number		
A3	LCD CONTROLLER		
Date: May 15, 1996		Sheet 12	of 1



CONFIDENTIAL

ACER ADVANCED LABS				
Title	PROJECT MARS MULTI-MEDIA			
Size A3	Document Number: LCD INTERFACE LOGICS			
Date:	May 9, 1996	Sheet 13	of	14

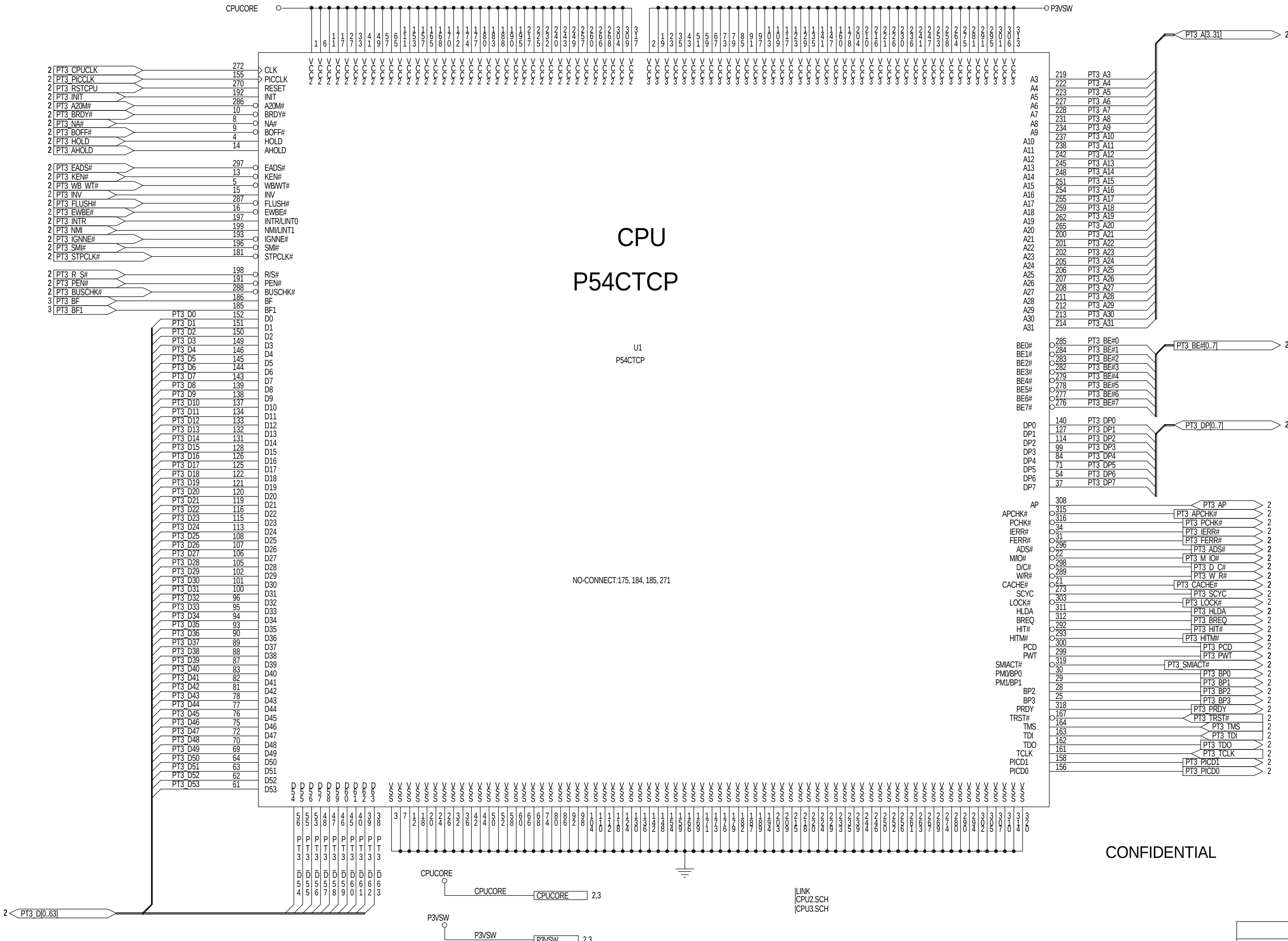


CONFIDENTIAL

ACER ADVANCED LABS	
Title	PROJECT MARS MULTI-MEDIA
Size A3	Document Number: LOGICS & SPARE GATES
Date: May 9, 1996	Sheet 14 of 14

This section shows the **CPU board** schematic diagrams of the notebook.

Schematics Page List:

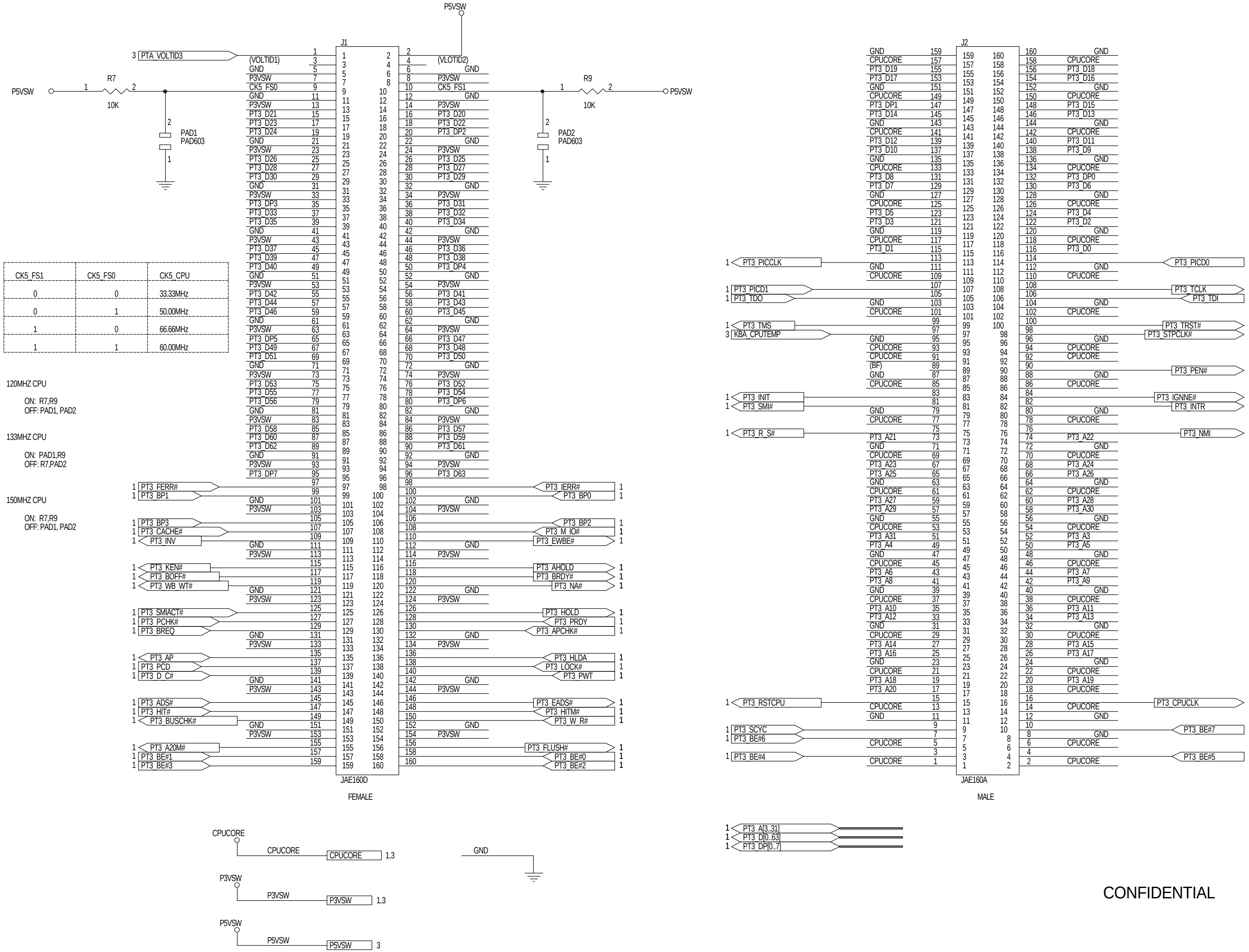


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ACER ADVANCED LABS

Title

P54C TCP CPU MODULE



CK5_FS1	CK5_FS0	CK5_CPU
0	0	33.33MHz
0	1	50.00MHz
1	0	66.66MHz
1	1	60.00MHz

120MHZ CPU

ON: R7,R9
OFF: PAD1, PAD2

133MHZ CPU

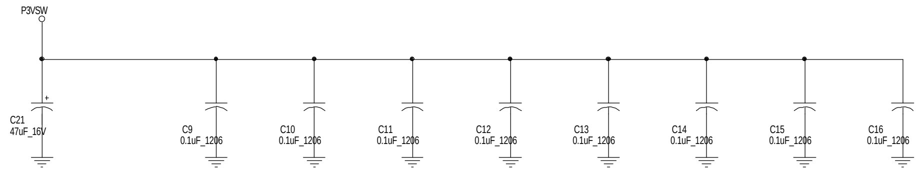
ON: PAD1,R9
OFF: R7,PAD2

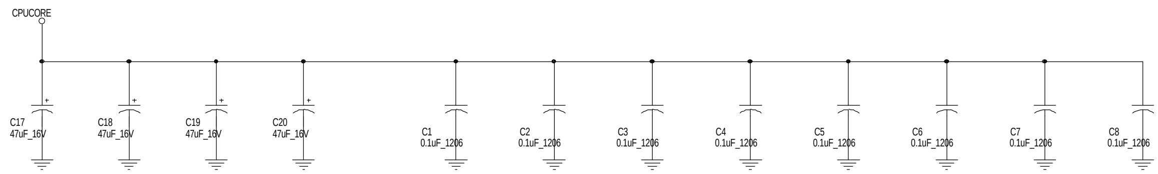
150MHZ CPU

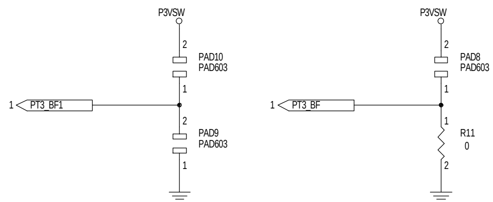
ON: R7,R9
OFF: PAD1, PAD2

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ACER ADVANCED LABS	
Title	P54C TCP CPU MODULE
Size A3	Document Number: CPU INTERFACE CONNECTOR
Date: April 8, 1996	Sheet 2 of 3



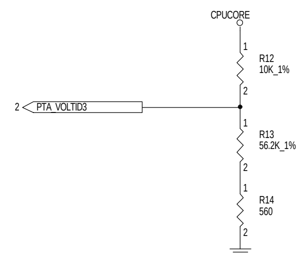


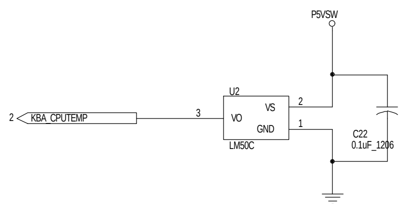


BUS FRACTION DEFINTION

BF1	BF	P54CS(A,B-STEP)	P54CS(C-STEP)	P55C
0	0	NOT DEFINED	2/5	2/5
0	1	NOT DEFINED	NOT DEFINED	NOT DEFINED
1	0	1/2 *	1/2 *	1/2
1	1	2/3	2/3	NOT DEFINED

*: DEFAULT SETTING IN THE MARS SYSTEM.

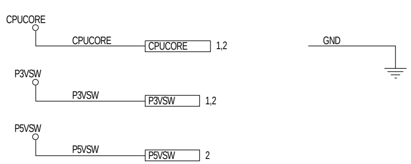


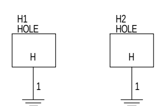


R13	R14	CPUCORE
OPEN	OPEN	2.5V
113K 1%	680 5%	2.7V
* 56.2K 1%	* 560 5%	2.9V
37.4K 1%	470 5%	3.1V
28K 1%	390 5%	3.3V

*: DEFAULT SETTING IN THE MARS SYSTEM.

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MOUNTING HOLES

	ACER ADVANCED LAB
Title	P54C TCP CPU MODULE
Size A3	Document Number
Date:	April 8, 1996 — Sheet 3 of 3

BIOS POST Checkpoints

This appendix lists the POST checkpoints of the notebook BIOS.

Table E-1 POST Checkpoint List

Checkpoint	Description
04h	• Determines if the current booting procedure is from cold boot (press reset button or turn the system on), from warm boot (press b +a+^), or from exiting BIOS setup. *Note: At the beginning of POST, port 64 bit 2 (8042 system flag) is read to determine whether this POST is caused by a cold or warm boot. If it is a cold boot, a complete POST is performed. If it is a warm boot, the chip initialization and memory test is eliminated from the POST routine.*
08h	• Disables Non-Maskable Interrupt (NMI), Alarm Interrupt Enable (AIE), Periodical Interrupt Enable (PIE), and Update-ended Interrupt Enable (UIE). *Note: These interrupts are disabled in order to avoid any mis-action happened during the POST routine.*
09h	• Initializes Vesuvius ChipSet V1-LS, V2-LS and V3-LS
10h	• DMA(8237) testing & initialization
14h	• System timer (8254) testing & initialization
18h	• Memory refresh test; refresh occurrence verification (IRQ0)
1Ch	• Verifies CMOS shutdown byte, battery and check sum *Note: Several parts of the POST routine require the system to be in protected mode. When returning to real mode from protected mode, the processor is reset, therefore POST is re-entered. In order to prevent re-initialization of the system, POST reads the shutdown code stored in location 0Fh in CMOS RAM. Then it jumps around the initialization procedure to the appropriate entry point.* • The CMOS shutdown byte verification assures that CMOS 0Fh area is fine to execute POST properly. • Initializes CMOS default setting • Initializes RTC time base *Note: The RTC has an embedded oscillator that generates 32.768 KHz frequency. To initial RTC time base, turn on this oscillator and set a divisor to 32768 so that RTC can count time correctly.*
1Dh	• DRAM type determination (FPM or EDO type)
1Eh	• DRAM sizing, 32/64 bit Memory Accessing
2Ch	• Tests 128K base memory *Note: The 128K base memory area is tested for POST execution. The remaining memory area is tested later.*

Table E-1 POST Checkpoint List

Checkpoint	Description
20h	• Tests keyboard controller (8041/8042) • Determines keyboard type (AT, XT, PS/2) then write default command byte upon KB type
23h	• Detects whether keyboard u is depressed from system powered-on till POST or not. If yes, set BIOS Setup parameter too default settings; or keep the original settings.
24h	• Tests programmable interrupt controller (8259) • Initializes system interrupt
30h	• Enables system shadow RAM
34h	• Memory sizing
56h	• Changes SMBASE, copy SMI Handler. • Issues 1st software SMI to communicate with PMU. • Initializes the SMI environment.
3Ch	• Initializes interrupt vectors
4Ch	• CPU clock checking • Sets the DRAM timing in correspondent to the system speed
35h	• Scans PCI Devices to Initialize the PCI buffer that used by BIOS.
4Eh	• Isolations for PnP ISA Card
4Fh	• Configurations for PnP ISA Card • Initializes the PCI device according to ESCD data (if ESCD data is valid). • Initialize the PCI Devices by BIOS • Initialize the PCI VGA card
50h	• Initializes video display *Note: If system has any display card, here it should be initialized via its I/O ROM or corresponding initialization program.*
Exh	• VGA BIOS POST.
54h	• Enables video shadow RAM
58h	• Displays Acer (or OEM) logo (if necessary) • Displays Acer copyright message (if necessary) • Displays BIOS serial number
5Ch	• Memory testing
60h	• External Cache sizing • Enables/disables L1/L2 cache according to the BIOS SETUP
64h	• Tests keyboard interface *Note: The keyboard LEDs should flash once.*

Table E-1 POST Checkpoint List

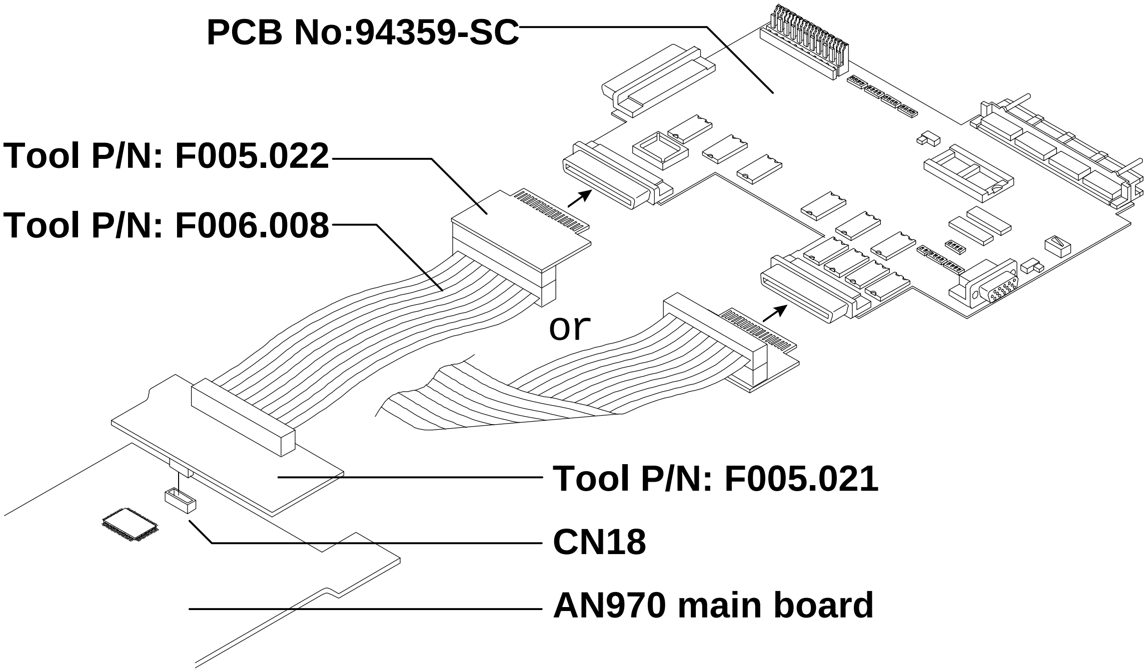
Checkpoint	Description
68h	• Enables UIE, then checks RTC update cycle *Note: The RTC executes an update cycle per second. When the UIE is set, an interrupt (IRQ8) occurs after every update cycle and indicates that over 999ms are available to read valid time and date information.*
70h	• Parallel port testing
74h	• Serial port testing
78h	• Math coprocessor testing
7Ch	• Reset pointing device
80h	• Set security status
84h	• KB device initialization • Set KB led upon setup requests • Enable KB device
86h	• Issue 2nd software SMI to communicate with PMU • Enable the use of BIOS Setup, system information. and fuel gauge
6Ch	• Tests and initializes FDD *Note: The FDD LED should flash once and its head should be positioned.*
88h	• HDD testing & parameter table setup • Initializes HDD enhanced features
90h	• Displays POST status if necessary • Changes POST mode to default text mode
94h	• Initializes I/O ROM *Note: I/O ROM is an optional extension of the BIOS located on an installed add-on card as a part of the I/O subsystem. POST detects I/O ROMs and gives them opportunity to initialize themselves and their hardware environment.* • Shadows I/O ROM if setup requests • Builds up free expansion ROM table
96h	• Initializes PCI Card ROM • Writes ESCD data into NVRAM
97h	• Writes ESCD data into NVRAM
A0h	• Initializes timer counter for DOS use
A4h	• Initializes security feature
ACh	• Enables NMI • Enables parity checking • Sets video mode
AEh	• Issues 3rd software SMI to communicate with PMU • Starts all power management timers • Checks whether system is resumed from 0V suspend or not.

Table E-1 POST Checkpoint List

Checkpoint	Description
B0h	• Power on password checking • Display configuration table • Clear memory buffer used for POST • Select boot device
BDh	• Shutdown 5
BEh	• Shutdown A
BFh	• Shutdown B

Debug Board Information

This appendix shows the model number definition of the notebook.



Ordering contact person: Michael Shieh (by CC:mail)

Ordering parts information:

PCB number	Tool part number	Descriptions
94369-SC	--	Notebook debug board[1]
--	F005.021	PC Board bridges M/B and cable
--	F006.008	Cable
--	F005.022	PC Board bridges cable and debug board

1 The debug board is same to the one used on AN950 machine.

Forms

This appendix contains forms that can help improve Acer service. Use these forms whenever necessary.

F.1 Reader Response Form

This form helps gauge the organization, the accuracy, and the completeness of the manual. It tells us if the manual is precise in its conveyance of the pertinent data, information, and facts concerning the unit.

F.2 Incoming Inspection Report

This form lists all the necessary information regarding the defective unit(s): the model number, invoice number, quantity involved. It also categorizes the line parameter of the defect, whether it is a major defect, a minor defect, or if it is within the acceptable range of functioning.

F.3 Field Maintenance Report

This form classifies the type of machine failure, whether the trouble lies within the motherboard, the video board, the controller, the storage devices, or elsewhere. It also lists the quantity percentage defect of the shipment to the distributor.

F.4 Problem Report Forms

The attached forms are for the user to explain any problem that may occur with an Acer product. Acer engineers can better understand the problem through the feedback of the user, whether electrical, mechanical, or electronic in nature.

Use of these forms saves time and effort in the repair process.

AcerNote 970
Reader Response Form

Dear Reader,

At Acer, documentation is not viewed as a necessary evil. On the contrary, documentation support, like product reliability and performance, has always been viewed as a potentially decisive factor for market success. Because documentation is important, we want to know what you think about our manuals. Please tell us by filling out and returning this Reader Response Card. Thanks for your help.

Company Name ____________________

Name: ____________________ **Occupation/Title:** ____________________

Address: ____________________

Telephone: ____________________ **Fax No.:** ____________________

Years of computer experience: ____________________

1. *How do you rate this manual?*

Effectiveness: *Is it organized so you can find things easily? Are the index and table of contents easy to use? Are topics complete, accurate, and useful?*

	Excellent	**Good**	**Fair**	**Poor**
Table of Contents	______	______	______	______
Index	______	______	______	______
Organization	______	______	______	______
Accuracy	______	______	______	______
Completeness	______	______	______	______

Writing and Layout: Is the writing clear and easy to understand? Is the tone friendly or patronizing? Does the technical level match your needs? Is the text easy to the eyes? Are the illustrations helpful?

Clarity	______	______	______	______
Design	______	______	______	______
Tone	______	______	______	______
Level	______	______	______	______
Fonts and sizes	______	______	______	______
Illustrations	______	______	______	______

Others:

Binding method	______	______	______	______
Size and weight	______	______	______	______
Material	______	______	______	______
Overall rating	______	______	______	______

2. *What did you like most about it? What would it take to make it better?*

____

Postage
Stamp
Here

Customer Support Division
Acer Incorporated
6F, 156 Min Sheng East Road, Sec. 3
Taipei 105, Taiwan, R.O.C.

Manual Title	***:***	***AcerNote 970 Service Guide***
Part No.	***:***	***49.46811.011***
Doc. No.	***:***	***SG230-9701A***

Date (mm/dd/yy): __________ Sheet ___ of ___

Acer Products
Incoming Inspection Report

Distributor: ________________________
Year/Month: _______________________

* Major defect : M * Minor defect : m * Acceptable : A

Model Number: __________________ Test Date (mm/dd/yy): __________________
Invoice Number: __________________ Remarks:
Qty. Received: __________________

Qty. Inspected: ________ = _____ %
(1) M : ________ sets = _____ %
(2) m : ________ sets = _____ %
(3) A : ________ sets = _____ %

Model Number: __________________ Test Date (mm/dd/yy): __________________
Invoice Number: __________________ Remarks:
Qty. Received: __________________
Qty. Inspected: ________ = _____ %
(1) M : ________ sets = _____ %
(2) m : ________ sets = _____ %
(3) A : ________ sets = _____ %

Model Number: __________________ Test Date (mm/dd/yy): _________________
Invoice Number: __________________ Remarks:
Qty. Received: __________________

Qty. Inspected: ________ = _____ %
(1) M : ________ sets = _____ %
(2) m : ________ sets = _____ %
(3) A : ________ sets = _____ %

Model Number: __________________ Test Date (mm/dd/yy): __________________
Invoice Number: __________________ Remarks:
Qty. Received: __________________

Qty. Inspected: ________ = _____ %
(1) M : ________ sets = _____ %
(2) m : ________ sets = _____ %
(3) A : ________ sets = _____ %

Model Number: __________________ Test Date (mm/dd/yy): __________________
Invoice Number: __________________ Remarks:
Qty. Received: __________________

Qty. Inspected: ________ = _____ %
(1) M : ________ sets = _____ %
(2) m : ________ sets = _____ %
(3) A : ________ sets = _____ %

Date (mm/dd/yy): __________ Sheet ___ of ___

Acer Products
Field Maintenance Report

Distributor: ________________________
Year/Month: _______________________

* Fixed after repair : F * Not fixed after repair : N

Model Number: __________________

Qty. Installed: __________________
Qty. Returned: ________ = _____ %

Qty. Repaired: ________ = _____ %
(1) F : ________ sets = _____ %
(2) N : ________ sets = _____ %

Failure Classification
Motherboard: _____ % Video board: ____ %
Controller: _____ % Storage device: ____ %
No problem found: _____ % Others: ____ %
Remarks:

Model Number: __________________

Qty. Installed: __________________
Qty. Returned: ________ = _____ %

Qty. Repaired: ________ = _____ %
(1) F : ________ sets = _____ %
(2) N : ________ sets = _____ %

Failure Classification
Motherboard: _____ % Video board: ____ %
Controller: _____ % Storage device: ____ %
No problem found: _____ % Others: ____ %
Remarks:

Model Number: __________________

Qty. Installed: __________________
Qty. Returned: ________ = _____ %

Qty. Repaired: ________ = _____ %
(1) F : ________ sets = _____ %
(2) N : ________ sets = _____ %

Failure Classification
Motherboard: _____ % Video board: ____ %
Controller: _____ % Storage device: ____ %
No problem found: _____ % Others: ____ %
Remarks:

Model Number: __________________

Qty. Installed: __________________
Qty. Returned: ________ = _____ %

Qty. Repaired: ________ = _____ %
(1) F : ________ sets = _____ %
(2) N : ________ sets = _____ %

Failure Classification
Motherboard: _____ % Video board: ____ %
Controller: _____ % Storage device: ____ %
No problem found: _____ % Others: ____ %
Remarks:

Model Number: __________________

Qty. Installed: __________________
Qty. Returned: ________ = _____ %

Qty. Repaired: ________ = _____ %
(1) F : ________ sets = _____ %
(2) N : ________ sets = _____ %

Failure Classification
Motherboard: _____ % Video board: ____ %
Controller: _____ % Storage device: ____ %
No problem found: _____ % Others: ____ %
Remarks:

PC/Peripheral Problem Report Form

Customer:____Date:______________________

Issue I.D.:______________________S/N:_____________________Attachment:________________

Model No.:______________________S/N:_____________________BIOS Version:______________

RAM Size:______________________O.S.:____________________EnE.Version:_________________

Add-On Cards:____

Disk Type & Capacity:____

Disk Controller:____

A/P Name & Version:____

Other: ____

Error Message: ____

Problem Description:

- CHARACTERISTICS:
- QUALITY ISSUE
- SPECIFICATION
- PERFORMANCE
- COMPATIBILITY

PROBLEM OCCURS:
- ONLY ONCE
- INTERMITTENTLY
- CONTINUOUSLY

- TIME OF FAILURE:
- INSTALLATION
- DURING OPERATION
- OTHERS

Assigned Product Engineer : ____________________________ Date Resolved:_________________

Comments:____

____

____

Multiuser Product Problem Report Form

Customer:____ Date:____________________

Issue I.D.:____________________ S/N:____________________ Attachment:______________

Model No.:____________________ S/N:____________________ BIOS Version:______________

RAM Size:____________________ O.S.:____________________ EnE.Version:______________

Add-On Cards:____

Disk Type & Capacity:____

Disk Controller:____

A/P Name & Version:____

Other: ____

Error Message: ____

Problem Description:

- CHARACTERISTICS:
- QUALITY ISSUE
- SPECIFICATION
- PERFORMANCE
- COMPATIBILITY

PROBLEM OCCURS:
- ONLY ONCE
- INTERMITTENTLY
- CONTINUOUSLY

- TIME OF FAILURE:
- INSTALLATION
- DURING OPERATION
- OTHERS

Assigned Product Engineer : ______________________________ Date Resolved:______________

Comments:____

____

____

LAN Product Problem Report Form

Customer:____________________ Date:____________________

Issue I.D.:____________ S/N:____________ Attachment:____________

Model No.:____________ S/N:____________ BIOS Version:____________

RAM Size:____________ O.S.:____________ EnE.Version:____________

Add-On Cards:______________________________

Disk Type & Capacity:______________________________

Disk Controller:______________________________

A/P Name & Version:______________________________

Other: ______________________________

Error Message: ______________________________

Problem Description:

CHARACTERISTICS:
- QUALITY ISSUE
- SPECIFICATION
- PERFORMANCE
- COMPATIBILITY
- CONNECTIVITY

TIME OF FAILURE:
- INSTALLATION
- DURING OPERATION
- OTHERS

PROBLEM OCCURS:
-ONLY ONCE
-INTERMITTENTLY
-CONTINUOUSLY

-TIME OF FAILURE:
-INSTALLATION
-DURING OPERATION
-OTHERS

CMOS SETUP:
SHADOW RAM:
BIOS RAM:
EMS MEMORY:
SPEED & CACHE
FDD/WDD TYPE:

Assigned Product Engineer : ____________________ Date Resolved:____________

Comments:______________________________

____

____